POWER SUPPLY CURRENT [$I_{PS}$] BASED TESTING OF CMOS AMPLIFIER CIRCUIT WITH AND WITHOUT FLOATING GATE INPUT TRANSISTORS

A Thesis

Submitted to the Graduate faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

in

The Department of Electrical and Computer Engineering

by
Vanikumari Pulendra
Bachelor of Engineering, Osmania University, 2001
December 2005
ACKNOWLEDGEMENTS

I dedicate this thesis to my parents, Mr. and Mrs. Pulendra and my sister Lakshmi and brother-in-law, for their constant prayers and steadfast support.

I am very grateful to my advisor Dr. A. Srivastava for his guidance, patience and understanding throughout this work. His suggestions, discussions and constant encouragement have helped me to get a deep insight in the field of VLSI design.

I would like to thank Dr. P. K. Ajmera and Dr. Martin Feldman for generously contributing their time, reading my thesis, providing important input and being a part of my committee.

I am deeply grateful to the staff and the faculty of ELRC, Chemistry and Electrical Engineering Departments, for supporting me financially during my stay at LSU.

I take this opportunity to thank my friends Siva, Pavan, Raghu and my roommates for their help and encouragement at times I needed them. I would also like to thank all my friends here who made my stay at LSU an enjoyable and a memorable one.

Last of all I thank GOD for keeping me in good health and spirits throughout my stay at LSU.
TABLE OF CONTENTS

ACKNOWLEDGEMENTS........................................................................................................... ii

LIST OF TABLES.................................................................................................................... v

LIST OF FIGURES.................................................................................................................. vi

ABSTRACT ............................................................................................................................... x

CHAPTER 1. INTRODUCTION .......................................................................................... 1
  1.1 TESTING METHODOLOGY....................................................................................... 4
  1.2 RESEARCH GOAL AND THESIS OVERVIEW ...................................................... 6

CHAPTER 2. MULTI INPUT FLOATING GATE (MIFG) MOSFETS ............................. 8
  2.1 STRUCTURE OF MIFG MOSFET AND DEVICE PHYSICS .................................... 8
  2.2 FLOATING GATE CMOS INVERTER ....................................................................... 11
  2.3 UNIT CAPACITANCE ............................................................................................. 13
  2.4 DESIGN ISSUES ....................................................................................................... 17

CHAPTER 3. DESIGN FOR TESTING A TWO STAGE CMOS OPERATIONAL AMPLIFIER .................................................................................................................... 18
  3.1 DESIGN OF A CMOS OPERATIONAL AMPLIFIER .............................................. 18
    3.1.1 A Two-Stage CMOS Amplifier Topology ......................................................... 20
      3.1.1.1 Current Mirrors ....................................................................................... 22
      3.1.1.2 Active Resistors ...................................................................................... 24
    3.1.2 Design of Operational Amplifier with Floating Gates at Input Stage .......... 27
      3.1.2.1 Capacitor Array Design ......................................................................... 34
      3.1.2.2 Biasing, Input and Second Gain Stages Design ......................................... 37
  3.2 COMPENSATION OF TWO-STAGE OP AMP ....................................................... 39

CHAPTER 4. I\text{PS} BASED TEST METHOD AND FAULT COVERAGE ...................... 46
  4.1 POWER SUPPLY CURRENT (I\text{PS}) TESTING PROCEDURE ............................ 46
    4.1.1 Physical Defects in CMOS Integrated Circuits ................................................. 47
      4.1.1.1 Bridging Faults ...................................................................................... 48
      4.1.1.2 Open Faults .......................................................................................... 50
      4.1.1.3 Fault Models, Simulation and Detection ................................................. 50
      4.1.1.4 Fault Injection Transistors ...................................................................... 51
    4.2 FAULT COVERAGE ............................................................................................... 54
      4.2.1 Simulated Amplifier Functional Testing Results .......................................... 64
      4.2.2 Simulated and Experimental I\text{PS} Testing Results ........................................ 70

CHAPTER 5. CONCLUSION .............................................................................................. 87

REFERENCES......................................................................................................................... 88
LIST OF TABLES

Table 3.1: Specifications of the designed op amps........................................................... 39
Table 4.1: Fault numbers related to node or transistor numbers for CUT 2....................... 60
Table 4.2: Fault numbers related to node or transistor numbers for CUT 3....................... 60
Table 4.3: SPICE simulated and experimental results for CUT 1...................................... 71
Table 4.4: SPICE simulated and experimental results for CUT 2...................................... 78
Table 4.5: SPICE simulated and experimental results for CUT 3...................................... 83
LIST OF FIGURES

Figure 1.1: An n-channel floating gate MOSFET [18]....................................................... 5

Figure 1.2: Block diagram of power supply current, $I_{PS}$ based testing............................... 6

Figure 2.1: Basic structure of a multi input floating gate MOSFET ...................................... 9

Figure 2.2: Terminal voltages and coupling capacitances of a multi input floating gate MOSFET. Note: the floating gate voltage is $\Phi_F$ ............................................. 10

Figure 2.3(a): MIFG p-MOSFET ..................................................................................... 12

Figure 2.3(b): MIFG n-MOSFET ..................................................................................... 12

Figure 2.4: Multi input floating gate (MIFG) CMOS inverter ............................................ 14

Figure 2.5: The capacitive network for a multi input floating gate CMOS inverter ......... 15

Figure 2.6: Transfer characteristics of a 4-input floating gate CMOS inverter ............ 16

Figure 3.1: Ideal operational amplifier ............................................................................. 19

Figure 3.2: Block diagram of an integrated operational amplifier ................................... 19

Figure 3.3: A two-stage CMOS operational amplifier without floating gate input transistors showing the aspect ratios of transistors ................................................. 21

Figure 3.4: Current mirror (a) p-MOS (b) n-MOS ........................................................... 23

Figure 3.5: Active resistors: (a) gate connected to drain and (b) gate connected to $V_{DD}$ 25

Figure 3.6: Layout of an operational amplifier design of the circuit of Fig 3.3. .......... 28

Figure 3.7: Post layout transfer characteristics of the circuit of Fig. 3.3......................... 29

Figure 3.8: Post layout simulated response of the CMOS amplifier circuit of Fig 3.6. ... 30

Figure 3.9: Post layout (Fig 3.6) simulated frequency response characteristics of the amplifier circuit of Fig 3.3. Note: The open loop gain is 81dB and the 3dB bandwidth is 1.1 kHz ................................................................. 31

Figure 3.10: Post layout (Fig 3.6) simulated (a) amplitude and (b) phase versus frequency response characteristics. Note: The phase margin is $77^0$ ........................................... 32
Figure 3.11: Post layout (Fig. 3.6) simulated slew rate characteristics of the amplifier circuit of Fig. 3.3. ........................................................................................................... 33

Figure 3.12: A two stage floating gate input CMOS op amp showing aspect ratios of the transistors designed.................................................................................................................. 35

Figure 3.13: A floating gate MOS differential pair [32].......................................................................................................................... 36

Figure 3.14: Layout showing the use of dummy capacitors to match the capacitors present at the corner of the capacitor array. .............................................................. 37

Figure 3.15: Layout of operational amplifier design of circuit of Fig. 3.12....................... 40

Figure 3.16: Post layout transfer characteristics of the circuit of Fig. 3.12....................... 41

Figure 3.17: Post layout simulated response of the CMOS amplifier circuit of Fig. 3.12. ................................................................................................. 41

Figure 3.18: Post layout (Fig. 3.15) simulated amplitude and phase versus frequency response characteristics. Note: The 3 dB gain and phase margin are 78 dB and 56°. .......................................................................................................................... 42

Figure 3.19: Post layout (Fig. 3.15) simulated slew rate characteristics of the amplifier circuit of Fig. 3.12...................................................................................... 42

Figure 3.20: Effect of pole-splitting capacitor on the gain and phase of an op amp. .... 44

Figure 3.21: Two-port network equivalent small signal model of a two-stage op amp configuration of Figs. 3.3 and 3.12 with an equivalent zero nulling resistance ($R_2$). ........................................................................................................... 45

Figure 4.1: Block diagram of power supply current, $I_{PS}$ based testing. .......................... 48

Figure 4.2: Drain-source, gate-source and inter-gate bridging faults in an inverter chain. .......................................................................................................................... 49

Figure 4.3: Bridging defects. ........................................................................................................ 49

Figure 4.4: Floating input and open MOSFET open circuit defects............................... 51

Figure 4.5 (a): n-MOS Fault injection transistor (FIT) used in the layout. ..................... 52

Figure 4.5 (b): Fault injection transistor between drain and source nodes of a CMOS inverter. .................................................................................................................... 53

Figure 4.6: Injected faults using FITs for circuit of Fig. 3.3. .............................................. 55
Figure 4.7: Layout of a two-stage CMOS amplifier circuit of Fig. 4.6 showing the defects induced in the CUT 1 using fault injection transistors ........................................... 56

Figure 4.8: A two stage floating gate input CMOS op amp showing node numbers. ...... 57

Figure 4.9: Layout of two stage CMOS amplifier with FG input transistors showing the short faults induced using FITs (CUT 2). ................................................................. 58

Figure 4.10: Layout of two stage CMOS amplifier with FG input transistors showing the open and short faults induced using FITs (CUT 3).............................................. 59

Figure 4.11(a): CMOS chip layout of a two-stage CMOS amplifier with out floating gate input transistors within a padframe of 2.25 mm × 2.25 mm size.................... 61

Figure 4.11(b): CMOS chip layout of a two-stage CMOS amplifier with floating gate input transistors and short faults within a padframe of 2.25 mm × 2.25 mm size. ................................................................................................................. 62

Figure 4.11(c): CMOS chip layout of a two-stage CMOS amplifier with floating gate input transistors and combined open and short faults within a padframe of 2.25 mm × 2.25 mm size................................................................................... 63

Figure 4.12(a): Microphotograph of the fabricated chip showing the CUT 1 (CMOS amplifier)......................................................................................................... 65

Figure 4.12(b): Microphotograph of the fabricated chip showing the CUT 2 (CMOS amplifier with floating gate input transistors and short faults)....................... 65

Figure 4.12(c): Microphotograph of the fabricated chip showing the CUT 3 (CMOS amplifier with floating gate input transistors and short faults)....................... 66

Figure 4.13(a): Output of the amplifier (CUT 1) for a sinusoidal input voltage of 100 mV p-p ................................................................................................................. 67

Figure 4.13(b): Output response of the amplifier (CUT 1) for an input sinusoidal p-p of 200 mV ........................................................................................................... 67

Figure 4.14: Post layout transient response of the CUT 3 ............................................ 68

Figure 4.15: Post layout frequency response of CUT 3............................................. 68

Figure 4.16(a): Operational amplifier as unity gain follower for CUT 2. ....................... 69

Figure 4.16(b): Operational amplifier as unity gain follower for CUT 3. ....................... 69
Figure 4.17: Post layout magnitude of $I_{PS}$ for no fault and seven injected short faults one at a time for CUT 1. .......................................................... 71

Figure 4.18 (i): $I_{PS}$ when No Fault, Faults 4 and 6 are injected one at a time for CUT1 . 72

Figure 4.18 (ii): $I_{PS}$ when Fault 1 is injected for CUT1 .............................................. 72

Figure 4.18 (iii): $I_{PS}$ when Fault 2 is injected for CUT1 .............................................. 73

Figure 4.18 (iv): $I_{PS}$ when Fault 3 is injected for CUT1 .............................................. 73

Figure 4.18 (v): $I_{PS}$ when Fault 5 is injected for CUT1. .............................................. 74

Figure 4.18 (vi): $I_{PS}$ when Fault 7 is injected for CUT1. .............................................. 74

Figure 4.19: Post layout magnitude of $I_{PS}$ for short faults (a) No fault through Fault 4 (b) Fault 5 through Fault 10, one at a time for CUT 2. .............................................. 76

Figure 4.19: Post layout magnitude of $I_{PS}$ for short faults (c) Fault 11 through 16 and (d) Fault 17 through Fault 22, one at a time for CUT 2. .............................................. 77

Figure 4.20 (i): $I_{PS}$ when No Fault is injected for CUT 2. .............................................. 79

Figure 4.20 (ii): $I_{PS}$ when Fault 1 is injected for CUT 2 .............................................. 79

Figure 4.20 (iii): $I_{PS}$ when Faults 7, 8,11,12,14 and 19 are injected for CUT 2 one at a time. ................................................................................................................ 80

Figure 4.20 (iv): $I_{PS}$ when Faults 14, 16, 18 and 19 are injected one at a time for CUT 2. ................................................................................................................ 80

Figure 4.21: Post layout magnitude of $I_{PS}$ for (a) No fault and Fault 1 through Fault 5 (Open Faults) (b) Fault 6 through Fault 12 (Short Faults). ......................... 82

Figure 4.22 (i): $I_{PS}$ when No Faults are injected for CUT 3.............................................. 83

Figure 4.22 (ii): $I_{PS}$ when Open Fault 1 is injected for CUT 3.............................................. 84

Figure 4.22 (iii): $I_{PS}$ when Open Fault 2 and 3 are injected for CUT 3. ......................... 84

Figure 4.22 (iv): $I_{PS}$ when Short Fault 1 and 2 are injected one at a time for CUT 3. ..... 85

Figure 4.22 (v): $I_{PS}$ when Short Fault 4 is injected for CUT 3.............................................. 85

Figure 4.22 (vi): $I_{PS}$ when Short Fault 7 is injected for CUT 3.............................................. 86
ABSTRACT

This work presents a case study, which attempts to improve the fault diagnosis and testability of the power supply current based testing methodology applied to a typical two-stage CMOS operational amplifier and is extended to operational amplifier with floating gate input transistors*. The proposed test method takes the advantage of good fault coverage through the use of a simple power supply current measurement based test technique, which only needs an ac input stimulus at the input and no additional circuitry. The faults simulating possible manufacturing defects have been introduced using the fault injection transistors. In the present work, variations of ac ripple in the power supply current $I_{PS}$, passing through $V_{DD}$ under the application of an ac input stimulus is measured to detect injected faults in the CMOS amplifier. The effect of parametric variation is taken into consideration by setting tolerance limit of $\pm 5\%$ on the fault-free $I_{PS}$ value. The fault is identified if the power supply current, $I_{PS}$ falls outside the deviation given by the tolerance limit. This method presented can also be generalized to the test structures of other floating-gate MOS analog and mixed signal integrated circuits.

*Part of the work presented is reported in a publication:

S. Yellampalli, A. Srivastava and V.K. Pulendra, “A combined oscillation, power supply current and $I_{DDQ}$ testing methodology for fault detection in floating gate input CMOS operational amplifier,” 48th IEEE Midwest International Symposium on Circuits, Cincinnati, Ohio, August 7-10, 2005 is in publication.
CHAPTER 1. INTRODUCTION

The increasing functional complexity and shrinking size of integrated circuits makes it very difficult to rule out faults during design and production, even with best available design tools and fabrication processes. Thus, testing plays an important role in the reduction of overall cost of a chip. Analog integrated circuits testing is much less structured and have been tested for critical specifications [1] e.g., ac gain over a range of frequencies, common-mode rejection ratio, signal-to-noise ratio, linearity, slew rate, due to the lack of simple fault models.

In the following, some of the testing methods are discussed. Wafer probe testing is used to detect faulty circuits [2, 3] in an early stage of integrated circuit fabrication and thus avoid expensive full specification testing and packaging on faulty circuits. Most of the methods proposed for fault detection require that a set of measurements must carefully be chosen [2, 3, 4] at wafer stage. Even if an optimal set of measurements can be chosen, it is difficult to deal with the limitation of the accessibility of the internal nodes in an integrated circuit. In some circumstances, the cost to develop adequate tests at wafer level would be high because of speed and number of output connections limitation. So further testing has to be done at chip level.

The functional testing usually results in longer test times because of redundant testing. It neither provides a good test quality nor a quantitative measure of test effectiveness or fault coverage. Reducing test time by optimizing the functional test set while achieving the desired parametric fault coverage has also been studied [5]. However, the technique needs a reasonably large number of sample circuits for collecting the test data.
Design for testability (DFT) is another widely used method [6]. Oscillation test strategy is based on the DFT technique [6, 7], gives good fault coverage and does not require any test vectors. In this method, the complex analog circuit is partitioned into functional building blocks such as an amplifier, comparator, Schmitt trigger, filter, voltage reference, oscillator, phase-locked loop (PLL), etc., or a combination of these blocks. During the test mode, each building block is converted into a circuit that oscillates. The oscillation frequency, $f_{\text{osc}}$ of each building block can be expressed as a function of its components values. However, the method suffers from performance degradation in complex integrated circuits since it is not usually possible to divide the circuit into the fundamental blocks.

Built-in self-test (BIST) method is based on measuring the output data and calculating the performance of the system using an on-chip circuitry [8, 9]. This method reduces testing complexity of mixed-signal integrated circuits by incorporating all or some of the testing circuitry on the silicon. An important component of a mixed-signal BIST is a precision analog signal generator required for on-chip stimulation. While the area overhead is kept to a minimum, these generators should be capable of synthesizing high-precision single and multitone signals with controllable frequency and amplitude. This method also suffers from performance degradation and does not cover a large number of physical defects.

Analog CMOS circuits have also been tested by varying the supply voltage in conjunction with the inputs [10]. This technique aims to sensitize faults by causing the transistors to switch between different regions of operation. A ramped power supply voltage has been used to test faults in op amp circuits. In ref [11], an ac supply voltage
has been used for improving the fault coverage. Although these techniques have achieved high fault coverage, the number of faults injected is quite small.

In analog circuits, the power supply current is a function of input signal, state of the circuit (faulty or faulty free) and value of the parameters of the circuit. The presence of fault in the circuit causes some degree of change in currents in some branches. Those changes in branch currents will result in a more or less significant change in the power supply current ($I_{PS}$) [12].

If changes in steady state or quiescent current ($I_{DDQ}$) is used for fault detection it is called (quiescent current) $I_{DDQ}$ testing. This is a well known testing technique for digital CMOS integrated circuits [13]. The test methodology based on the observation of the quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts and bridging faults. These defects are neither well modeled by the classical fault models nor detectable by conventional logic tests. In addition, $I_{DDQ}$ testing can be used as a reliability predictor due to its ability to detect defects that do not yet involve faulty circuit behavior but could be transformed into functional failures at an early stage of circuit life. Thus, $I_{DDQ}$ testing became a powerful complement to the conventional logic testing. The $I_{DDQ}$ testing method is applied to testing of analog CMOS integrated circuits also. However, CMOS analog circuits have the large quiescent current, which affects the fault detection using this method [14]. For fault detection by the $I_{DDQ}$ testing, the defective current should be at least an order of magnitude higher than the fault free current.

In testing of analog circuits, the tolerance on the circuit parameters has to be considered because this can result in a significant difference between the power supply
current of a manufactured circuit and its nominal value. So a fault free circuit can be considered as fault and a faulty as a fault free [12]. This problem is overcome in the present work by considering a tolerance limit of ± 5 % on the fault free $I_{PS}$ value such that it takes into account variations due to significant technology and design parameters.

The validity of $I_{PS}$ based testing methodology is extended for fault detection in CMOS op amp with floating gate input transistors. The floating gate MOSFET (FGMOS) was proposed in the year 1991 by Shibata and Ohmi [15] with enhanced functionality in comparison with a conventional MOSFET. Floating gate transistors have been extensively used to store digital information in EPROMs and EEPROMs. Recently, these gained prominence in analog and mixed signal design applications. Because of their reliable analog charge storage and programmable threshold voltage capabilities they are used in low voltage operational amplifiers, biquad filters, digital to analog converters, analog memory cell arrays [16, 17]. In floating gate MOSFETs, inputs are capacitively coupled to floating gate using poly-poly capacitors between each input and floating gate as shown in the Fig. 1.1 [18]. $C_1$ and $C_2$ are the input capacitors for the floating gate MOSFET. Charge on the floating gate is controlled by these inputs. In low power analog signal processing, signal swing is limited by the relatively high threshold voltage compared with the supply voltage. Floating gate MOSFETs can be used to overcome this limitation.

1.1 Testing Methodology

A CMOS operational amplifier has been considered for the applicability of the method since it is one of the commonly used building blocks in analog and mixed signal
integrated circuits. In analog circuits, the power supply current is a function of input signal, state of the circuit (faulty or fault-free) and value of the parameters of the circuit. In the present work, variations of ac ripple in the power supply current $I_{\text{PS}}$, passing through $V_{\text{DD}}$ under the application of an ac input stimulus is measured to detect injected faults in the CMOS amplifier. Figure 1.2 shows the block diagram of this method of testing. A small resistor is used to measure the voltage corresponding to power supply current. The resistor does not affect the performance of the circuit under test. A variation of ac ripple in the power supply current through $V_{\text{DD}}$ is measured with and without injected faults with a periodic pulse input. Input signal to the CUT should produce a noticeable amount of difference between the power supply current of each faulty case and fault-free case. A tolerance limit for the magnitude of $I_{\text{PS}}$ with no injected faults is defined as $\pm 5\%$, such that it will take into account the deviations of significant technology and design parameters. The magnitudes of ac ripple in the power supply current, $I_{\text{PS}}$ is also
determined with every injected fault. If the $I_{PS}$ value falls out of the tolerance limit the fault is detected. The validity of this testing methodology is extended for fault detection in CMOS op amp with floating gate input transistors.

![Block diagram of power supply current, $I_{PS}$ based testing.](image)

**Figure 1.2:** Block diagram of power supply current, $I_{PS}$ based testing.

### 1.2 Research Goal and Thesis Overview

The goal of this thesis was to cost effectively detect possible manufacturing defects in CMOS operational amplifier using the power supply current, $I_{PS}$ based testing method. In the following chapters, circuit design and technology considerations, the test methodology, transient simulations, post layout measurements and experimental results are discussed.
Chapter 2 explains the basic structure and operation of floating gate MOSFETs.

Chapter 3 presents design of CMOS op amp with and without floating gate input transistors.

Chapter 4 explains concept and implementation of power supply current ($I_{PS}$) based testing and describes simulation results of CUT. Experimental results of the fabricated circuits were presented, compared with simulation results.

Chapter 5 provides a summary of the work presented.

The MOS model parameters used for design is presented in Appendix A. The chip testing procedure is presented in Appendix B.
CHAPTER 2. MULTI INPUT FLOATING GATE (MIFG) MOSFETS

Floating gate MOSFET (FGMOS) is a conventional MOSFET except that the gate, which is built on the conventional poly 1, is floating. The multi-input floating gate (MIFG) MOSFET is a transistor that switches to an ON or OFF state depending on the weighted sum of all input signals applied at its input node which are capacitively coupled to the gate. This leads to negligible amount of charging and discharging currents and ultimately leading to low power dissipation. Besides simple implementation of linear weighted voltage addition and analog memory capabilities, the other appealing features offered by MIFG transistor circuits are low voltage rail to rail operation, linearity improvement and with rail to rail swings [19].

2.1 Structure of MIFG MOSFET and Device Physics

The structure of multi input floating gate MOSFET comprises of the floating gate and number of input gates built on poly 2, which is coupled to poly 1 gate by capacitors between poly 1 and poly 2. The basic structure of the MIFG MOSFET is schematically illustrated in Fig 2.1 [20]. FGMOS can have more than one of the control gates, resulting in a multiple input MOSFET [15]. The floating gate in the MOSFET extends over the channel and the field oxide. A number of control gates, which are inputs to the transistor, are formed over the floating gate using the second poly-silicon layer (poly 2). In a floating gate transistor the charge on the gate of a MOSFET is controlled by two or more inputs through poly-poly capacitors between each input and the floating gate. The capacitive coupling between the multi-input gates and the floating gate and the channel is shown in Fig. 2.2, where $C_1$, $C_2$…$C_n$ are the coupling capacitors between the floating gate
and the inputs. The corresponding terminal voltages are \( V_1, V_2, V_3, \ldots, V_n \), respectively. \( C_0 \) is the capacitor between the floating gate and the substrate. \( V_{SS} \) is the substrate voltage.

At any time \( t \), the net charge \( Q_F(t) \) on the floating gate is given by the following equations [15, 20].

\[
Q_F(t) = Q_0 + \sum_{i=1}^{n} (-Q_i(t)) = \sum_{i=0}^{n} C_i(\Phi_F(t) - V_i(t)) \tag{2.1}
\]

or

\[
Q_F(t) = \Phi_F(t) \sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i(t) \tag{2.2}
\]

where \( n \) is the number of inputs, \( Q_0 \) is the initial charge present on the floating gate, \( Q_i(t) \) is the charge present in capacitor \( C_i \) and \( \Phi_F(t) \) is the potential at the floating gate. The potential of the floating gate \( \Phi_F \) is determined as...
Figure 2.2: Terminal voltages and coupling capacitances of a multi input floating gate MOSFET. Note: the floating gate voltage is $\Phi_F$.

\[
\Phi_F = \frac{C_1 V_1 + C_2 V_2 + \ldots + C_n V_n}{\sum_{i=0}^{n} C_i}
\]  

(2.3)

\[
\Phi_F(t) = \frac{\sum_{i=1}^{n} C_i V_i(t)}{\sum_{i=0}^{n} C_i}
\]  

(2.4)

Here, the substrate potential and the floating gate charge are assumed to be zero for simplicity. The equation (2.4) is obtained as follows:

Setting $V_{ss}$ to 0 and applying the law of conservation of charge at the

\[
\Phi_F(0)\sum_{i=0}^{n} C_i - \sum_{i=1}^{n} C_i V_i(0) = \Phi_F(t)\sum_{i=0}^{n} C_i - \sum_{i=1}^{n} C_i V_i(t)
\]  

(2.5)
or

\[
\Phi_F(t) \sum_{i=0}^{n} C_i - \Phi_F(0) \sum_{i=1}^{n} C_i = \sum_{i=0}^{n} C_i V_i(t) - \sum_{i=1}^{n} C_i V_i(0) \quad (2.6)
\]

or

\[
\Phi_F(t) = \Phi_F(0) + \frac{\sum_{i=1}^{n} C_i V_i(t) - \sum_{i=1}^{n} C_i V_i(0)}{\sum_{i=0}^{n} C_i} \quad (2.7)
\]

Assuming zero initial charge on the floating gate in Eq. (2.1), Eq. (2.7) reduces to

\[
\Phi_F(t) = \frac{\sum_{i=1}^{n} C_i V_i(t)}{\sum_{i=0}^{n} C_i} \quad (2.4)
\]

When the value of \( \Phi_F \) exceeds \( V_{th} \), the threshold voltage on floating gate, the transistor turns on. Thus the “ON” and “OFF” states of the transistor are determined whether the weighted sum of all input signal is greater than \( V_{th} \) or not. The behavior is quite analogous to that of biological neurons [15], and hence called neuron MOSFET or \( \nu \)MOSFET. The value of \( \Phi_F \) determined by Eq. (2.4) holds true, as long as all the input capacitive coupling co-efficient remain unchanged during the device operation. The oxide capacitance \( C_0 \) is assumed to remain constant. Figure 2.3 (a-b) shows the symbols of multi-input floating gate MOSFET of both p and n channel types.

2.2 Floating gate CMOS Inverter

A multi input floating gate CMOS inverter is shown in Fig. 2.4. From the Fig. 2.4, \( V_1, V_2, V_3, V_4, \ldots, V_n \) are input voltages and \( C_1, C_2, C_3, C_4, \ldots, C_n \) are corresponding input capacitors. To determine the voltage on the floating gate of the inverter Eq. (2.4) is used.
Figure 2.3: (a) MIFG p-MOSFET and (b) MIFG n-MOSFET.

Weighted sum of all inputs is performed at the gate and is converted into a multiple-valued input voltage, $V_{in}$ at the floating gate. The switching of the CMOS inverter depends on whether $V_{in}$ obtained from the weighted sum, is greater than or less than the
inverter threshold voltage or inverter switching voltage ($\Phi_{in}$). The switching voltage is computed from the voltage transfer characteristics of a standard CMOS inverter and is given by the following equation [21]

$$\Phi_{inv} = (\Phi_{go} + \Phi_{s1})/2$$  \hspace{1cm} (2.9)

where $\Phi_{go}$ and $\Phi_{s1}$ are the input voltages at which $V_{out}$ is $V_{DD} - 0.1$ V and 0.1 V, respectively. Hence the output ($V_{out}$) of a multi-input CMOS inverter is

$$V_{out} = \text{HIGH (3V)} \text{ if } \Phi_F < \Phi_{inv}$$

$$= \text{LOW (0V)} \text{ if } \Phi_F > \Phi_{inv}$$  \hspace{1cm} (2.10)

The capacitive network in an n-input CMOS inverter is shown in Fig. 2.5 [22]. The gate oxide capacitance of a p-MOSFET, $C_{oxp}$ is between the floating gate and n-well and is connected to $V_{DD}$. $C_p$ is the capacitance formed between poly silicon and the substrate connected to $V_{SS}$. The voltage on the floating gate is given by in an earlier work [22] and the analysis is presented. Figure 2.6 shows the circuit diagram and the transfer characteristics of a 4-input CMOS inverter as an illustration of Eq. (2.10).

The uniqueness of multi-input floating gate inverter lies in the fact that the switching voltage can be varied. Ordinarily, varying the $W_p/W_n$ ratios of the inverter does the threshold voltage adjustment. However, in multi input floating gate inverter, the varying coupling capacitances to the gate can vary the switching point in the DC characteristics.

### 2.3 Unit Capacitance

The floating gate CMOS circuit design layout faces certain shortcomings in fabrication process. Due to fabrication process variations in runs employed, designed capacitors may not turn out to be of right values since capacitors are expressed in integral multiples of a unit size capacitor. The capacitance parameter between poly 1 and poly 2
Figure 2.4: Multi input floating gate (MIFG) CMOS inverter.
Figure 2.5: The capacitive network for a multi input floating gate CMOS inverter [22].
Figure 2.6: Transfer characteristics of a 4-input floating gate CMOS inverter.
layers in 1.5 µm standard CMOS process [23] varies from 570 aF/µm² to 620 aF/µm² for different runs. Since we do not have prior knowledge of which run would be used in fabrication of our chip we have used 596 aF/µm².

2.4 Design Issues

Simulation techniques used for multi input floating gate CMOS circuits are different from a standard CMOS inverter. Simulation using SPICE gives the problem of DC convergence. It views the capacitors as open circuits initially and stops the simulation run. To overcome the problem different approaches have been explained in [24, 25, 26]. These techniques employ additional use of resistors and voltage controlled voltage sources for specifying the initial floating gate voltage.
CHAPTER 3. DESIGN FOR TESTING A TWO STAGE CMOS OPERATIONAL AMPLIFIER

A CMOS operational amplifier or op amp has been considered for the applicability of the power supply current based testing method since it is one of the most commonly used building blocks in analog and mixed-signal integrated circuits. If the amplifiers are proven to be fault free, the fault coverage would significantly be improved. In this chapter the design and the stability of the operational amplifier with and without floating gate input transistors are presented.

3.1 Design of a CMOS Operational Amplifier

An op amp has ideally infinite differential voltage gain, infinite input resistance, and zero output resistance. In reality, it only approaches these values. A conceptual block diagram of two stage op amp is shown in Fig. 3.1. Circuits made from op amps and a few passive components can be used to realize variety of important functions as summing and inverting amplifiers, integrators, and buffers. The combination of these functions and comparators can result in many complex functions, such as high-order filters, signal amplifiers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, input and output signal buffers, and many more.

Characteristics of high performance operational amplifier are high open loop gain, high bandwidth, very high input impedance, low output impedance and an ability to amplify differential-mode signals to a large extent and at the same time, severely attenuate common-mode signals. The operational amplifier design consists of three functional building blocks as depicted in Fig. 3.2. First, there is an input differential gain stage that amplifies the voltage difference between the input terminals, independently of
Figure 3.1: Ideal operational amplifier.

Figure 3.2: Block diagram of an integrated operational amplifier.
their average or common-mode voltage. Most of the critical parameters of the op amp like the input noise, common-mode rejection ratio (CMRR) and common-mode input range (CMIR) are decided by this stage. The differential to single-ended conversion stage follows the differential amplifier and is responsible for producing a single output, which can be referenced to ground. The differential to single-ended conversion stage also provides the necessary bias for the second gain stage. Finally, additional gain is obtained in the second gain stage which is normally a common-source gain stage that has an active load. Capacitor, \( C \) is included between the differential and the common-source stages to ensure stability when the amplifier is used with feedback. An output stage can be added to provide a low output resistance and the ability to source and sink large currents, but in this design we are not employing it since it is not necessary in the present work. In the following subsections, the description as well as the design methodology of each of the stages mentioned above is presented.

3.1.1 A Two-Stage CMOS Amplifier Topology

Figure 3.3 shows the circuit diagram of a two-stage, internally compensated CMOS amplifier used for the testing, which is adapted from the work of Alli [27]. The circuit provides good voltage gain, a good common-mode range and good output swing. Before the analysis of the op amp is done, some of the basic principles behind the working of MOS transistors are reviewed. The first stage in Fig. 3.3 consists of a p-channel differential pair \( M_1-M_2 \) with an n-channel current mirror load \( M_3-M_4 \) and a p-channel tail current source \( M_5 \). The second stage consists of an n-channel common-source amplifier \( M_6 \) with a p-channel current source load \( M_7 \) and the high output resistances of these two transistors equate to a relatively large gain for this stage and
an over all moderate gain for the complete amplifier. Because the op amp inputs are connected to the gates of MOS transistors, the input resistance is essentially infinite when the amplifier is used in internal applications. The sizes of the transistors were designed for a bias current of 100 µA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.
3.1.1.1 Current Mirrors

Current mirrors are used extensively in MOS analog circuits both as biasing elements and as active loads to obtain high AC voltage gain [28,29,30]. Enhancement mode transistors remain in saturation when the gate is tied to the drain.

\[ V_{DS} > V_{GS} - V_{th} \]  \hspace{1cm} (3.1)

Based on Eq. (3.1), constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor. Figures 3.4(a) and (b) show the p-MOS and n-MOS current mirrors design. A p-MOS mirror serves as a current source while the n-MOS acts as a current sink. The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, the currents when both transistors are in the saturation region of operation, are governed by the following Eq. (3.2) assuming matched transistors. The current ratio \( I_{OUT}/I_{REF} \) is determined by the aspect ratios of the transistors. The reference current that was used in the design is 100 µA. The desired output current is 200 µA. For the p-MOS current mirror, we can write,

\[ \frac{I_{OUT}}{I_{REF}} = \frac{(W_7/L_7)}{(W_8/L_8)} \]  \hspace{1cm} (3.2)

For \( (W_7/L_7)/ (W_8/L_8) = 2 \),

\[ I_{OUT} = 2 \times I_{REF} \cong 200 \, \mu A \]  \hspace{1cm} (3.3)

For identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to process variations, the accurate ratios usually result when devices of the same channel length are used, and the ratio of currents is set by the channel width.
Figure 3.4: Current mirror (a) p-MOS (b) n-MOS transistors.
For the n-MOS current mirror design shown in Fig. 3.4(b),

\[
\frac{I_{\text{OUT}}}{I_{\text{REF}}} = \frac{(W_4/L_4)}{(W_3/L_3)}
\]  

(3.4)

For \((W_4/L_4)/(W_3/L_3) = 1\),

\[
I_{\text{OUT}} = I_{\text{REF}} \approx 50 \mu\text{A}
\]  

(3.5)

### 3.1.1.2 Active Resistors

There are two active resistors used in the design. Firstly, the reference current that is applied to the current mirror is obtained by means of an active resistor. The resistor here is obtained by simply connecting the gate of a MOSFET to its drain as shown in Fig. 3.5(a). This connection forces the MOSFET to operate in saturation in accordance with the equation,

\[
I_{DS} = \frac{\beta (V_{GS} - V_{th})^2}{2}
\]  

where \(\beta\) is the transconductance parameter, \(V_{th}\) is the threshold voltage and \(V_{GS}\) is the gate-source voltage. Since the gate is connected to the drain, current \(I_{DS}\) is now controlled directly by \(V_{DS}\) and therefore the channel transconductance becomes the channel conductance. The small signal resistance is given by

\[
r_{\text{out}} = \frac{r_{ds}}{1 + g_m r_{ds}} \approx \frac{1}{g_m}
\]  

(3.7)

where \(g_m\) is the transconductance of the MOS transistor. It is described by the following equation.

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{V_{DS,\text{constant}}} = \sqrt{2\beta I_D}
\]  

(3.8)

It is to be noted that the transconductance of a MOS transistor increases as the square root of the drain current. Hence, MOS amplifiers need several stages to achieve large gains.
The second active resistor shown in Fig 3.5(b) has been used to realize the nulling resistance to reduce the effects of the right hand plane zero in the transfer function. The gate of this transistor M_{11} is biased at V_{DD}. Its small signal output resistance is obtained from Eq (3.7).

The small signal gain of the amplifier stage of Fig. 3.3 is described as follows [31],

\[
A_1 = g_m \left( r_{o2} \parallel r_{o4} \right) = \frac{2\sqrt{\beta}}{(\lambda_2 + \lambda_4)I_{SS}} = \frac{2}{(\lambda_2 + \lambda_4)(V_{GS} - |V_{th,p}|)}
\]  

(3.9)

where I_{SS} is the differential amplifier bias current and |V_{th,p}| is the threshold voltage of the p-MOS transistors forming the differential pair. The differential pair needs to be biased by a constant current source, which is provided by the 100 \mu A current source. The same current is supplied to the two stages of the operational amplifier by the p-channel current mirrors M_8, M_7, M_5 which provide the bias current for the two stages. In the differential amplifier stage, differential amplification is accomplished and differential to single-ended conversion is done. Thus, the output is taken only from one of the drains of the transistors. The n-channel devices M_3 and M_4 which are the load for the p-channel

Figure 3.5: Active resistors: (a) gate connected to drain and (b) gate connected to V_{DD}.
devices, also aid in the single-ended conversions. The second stage provides the additional gain. It is once again biased by a current source, which is also used to maximize the gain of the second stage. To get a high gain with reasonable high output resistance, the minimum channel length used is 3.2 µm and the maximum width of the transistor used is 235.6 µm. Transistor M$_6$ is critical to the frequency response, is biased at $I_{D6} = 200 \mu A$ and has $(W/L)_6 = (W/L)_{max} \approx 22$. The second stage is biased at $-I_{D7} \approx 200 \mu A$ to avoid input offset voltage. Transistors M$_3$ and M$_4$ are dimensioned according to

$$\frac{(W/L)_6}{2 \times (W/L)_{3,4}} = \frac{I_{D7}}{I_{D5}} = \frac{200 \mu A}{100 \mu A} = 2 \rightarrow \left( \frac{W}{L} \right)_{3,4} = \frac{1}{4} \left( \frac{W}{L} \right)_6 \approx 5.5$$

Choose the smallest device length that will keep the channel modulation parameter constant and give good matching for current mirrors. The channel length is chosen to be $L = 3.2 \text{ µm}$. Therefore, $W = 17.6 \text{ µm}$ for the transistors M$_3$ and M$_4$. To obtain the bias current of 50 µA, a MOS transistor is used with appropriate value of width (which is the MOSFET simulating resistors). Large W/L ratios for the transistors in the operational amplifier are obtained by using the unit matching principle where multiple numbers ($n$) of transistors are connected in such a way that the effective W/L ratio is $n$ times the W/L ratio of each transistor. The technique reduces the required area, in comparison to a device laid out in a straight forward manner. The benefit of this technique is reduced junction capacitance, and is well characterized [28].

The physical layout of the amplifier was made using the L-EDIT 8.3 and the ‘spice’ netlist extracted including parasitic capacitances. The layout of the amplifier is shown in the Fig 3.6. The value of the compensating capacitor, $C_C$ used in the layout is 2 pF, whose area (46.4 x 52.8 µm$^2$) has been designed using the area capacitance ($C' = 596$
aF/µm²) between the poly and poly2 layers provided by MOSIS [23]. The need for stabilization of op amp using Cc and M11 is discussed in Section 3.2. Figure 3.7 shows the simulated transfer characteristics using MOS level-3 model parameters [23], obtained from DC sweep analysis. The maximum input range is ±100 mV. Figure 3.8 shows the transient analysis for a sinusoidal input with peak-to-peak amplitude of 200 mV applied to the inverting terminal of the operational amplifier at a frequency of 500 kHz. An inverted waveform is obtained at the output of the op amp with peak-to-peak amplitude of 4.6 V, giving a voltage gain of 23 at 500 kHz. Figure 3.9 shows the frequency response characteristics. The 3 dB bandwidth of the amplifier obtained is approximately 1.1 kHz and the 3 dB gain is 78 dB. The output offset voltage calculated from the transfer characteristics is 20.6 mV. With an open-loop gain of 81 dB, the input offset voltage is approximately 1.8 µV. Figure 3.10(a) shows the amplitude versus frequency behavior. Figure 3.10(b) shows the phase versus frequency characteristics. The phase noise margin calculated at 0 dB is 77°. The slew rate of the operational amplifier is 46 V/µs as shown in Fig 3.11.

3.1.2 Design of Operational Amplifier with Floating gates at Input Stage

The design of op amp shown in Fig. 3.12 is similar to the op amp shown in Fig. 3.3 except that its input stage has floating gate MOS transistors. The advantage of using FGMOS transistors in the design of operational amplifier as follows:
Figure 3.6: Layout of an operational amplifier design of the circuit of Fig. 3.3.
DC Input Offset Voltage = 1.8µV

Figure 3.7: Post layout transfer characteristics of the circuit of Fig. 3.3.
Figure 3.8: Post layout simulated response of the CMOS amplifier circuit of Fig. 3.6.
3dB Band Width = 1.1 KHz

3dB Gain = 81dB – 3 dB = 78dB

Figure 3.9: Post layout (Fig. 3.6) simulated frequency response characteristics of the amplifier circuit of Fig. 3.3. Note: The open loop gain is 81dB and the 3dB bandwidth is 1.1 kHz.
Figure 3.10: Post layout (Fig. 3.6) simulated (a) amplitude and (b) phase versus frequency response characteristics. Note: The phase margin is $77^\circ$. 

Phase margin = $77^\circ$
Figure 3.11: Post layout (Fig. 3.6) simulated slew rate characteristics of the amplifier circuit of Fig. 3.3.
To sustain a constant transconductance from a simple differential pair, the common mode input voltage has to be adequately far above ground so that the gate-to-source voltage of the input transistors would be large enough to pass a significant fraction of $I_b$ as shown in Fig. 3.13 [32] and so that the transistor that sinks the bias current remains in saturation. For bias currents at or near threshold, the input common-mode voltage must remain greater than $V_{th} + V_{DSsat}$, where $V_{DSsat}$ is the drain to source voltage of a MOSFET in saturation region [32]. One method to overcome the limitation is by using the floating gate MOS (FGMOS) transistors. The property of adjustable threshold voltages of the FGMOS transistors by adjusting the amount of charge, $Q$, stored on the gates of these devices effectively makes them to depletion mode devices. In this case, the common mode control gate input voltage can be at ground while the common mode floating-gate voltage is higher than $V_{th} + V_{DSsat}$, permitting proper operation of the differential pair. We can increase the charge on the floating gates by adding an extra control gate to each FGMOS transistor.

3.1.2.1 Capacitor Array Design

The floating gate transistor uses 512 fF capacitor each at its input which has been designed in an integer multiple of 256 fF unit size capacitor. Figure 3.14 shows the layout of the capacitor array designed. The array is surrounded with dummy capacitors and guarded by the guard ring to cancel out the effect of parasitics. The capacitors, which are present at the end of the arrays, do not have the surrounding capacitors to cancel out the relative error. To take care of these capacitors dummy capacitors are added to the array [31, 33]. The use of dummy capacitors in the capacitor array layout is shown in Fig 3.14. The substrate noise present in the substrate can be coupled to the capacitor through its
The parasitic capacitor and any voltage variation present is also coupled to other components of the chip. To avoid this coupling the capacitor array is shielded from the substrate with N-well under it and connecting it to a quiet DC potential [33]. The guard rings (n^+) are used in the layout around the capacitor array to prevent from any sort of interference. A common centroid layout scheme is employed in the design.

Figure 3.12: A two stage floating gate input CMOS op amp showing aspect ratios of the transistors designed.
Figure 3.13: A floating gate MOS differential pair [32].
3.1.2.2 Biasing, Input and Second Gain Stages Design

As discussed earlier, all the transistors are assumed to be in saturation and neglect the channel length modulation effects. To avoid channel length modulation the channel length is usually increased instead of keeping it at minimum feature size. The differential amplifier needs to be biased by a constant current source, which is provided by the M10 transistor. This current is supplied to the two stages of the operational amplifier by the p-channel current mirrors M8, M5, M7 which provide the bias current for the two stages. In the differential amplifier stage the differential to single ended conversion is also done...
which makes the output to be taken only from one of the drains of the transistors.

Transistor M5 is biased at \( I_{D5} = 50 \ \mu A \) resulting an aspect ratio \( (W/L)_5 = (W/L)_{\text{max}} \approx 37 \).

The input pair is biased at \( -I_{D7} = 100 \ \mu A \). To avoid input offset voltage transistors M3 and M4 are dimensioned according to

\[
\left( \frac{W}{L} \right)_6 = \frac{I_{D7}}{2 \times I_{D5}} = \frac{200 \mu A}{2 \times 100 \mu A} = 2 \rightarrow \left( \frac{W}{L} \right)_{3,4} = \frac{1}{4} \left( \frac{W}{L}_6 \right)
\]

(3.11)

Therefore the \( W = 19.2 \ \mu m \) for the transistors M3, M4. The n-channel transistors M3 and M4 acts as load for the p-channel transistors and are used for the single ended conversion also. The second stage of the op amp provides the additional gain and also the level shift for the output. The second stage is also biased by a current source, which is used to maximize the gain of the second stage. The op amp device sizes are chosen to get a high gain with high output resistance. The maximum width of the transistors in the op amp design is 235.6 \( \mu m \) and the minimum channel length used in the design is 3.2 \( \mu m \). The overall gain of the amplifier is

\[
A_v = A_{v1} A_{v2} = g_{m1} (r_{02} || r_{04}) g_{m6} (r_{06} || r_{05}) \approx (g_m r_0)^2
\]

(3.12)

The concept of stabilization of op amp is discussed in Section 3.2. The operational amplifier is made stable by using the compensation capacitor. The capacitor introduces a dominant pole and decreases the gain so that the phase margin is positive. Phase margin is defined as how far the phase of the circuit is away from 180° at a gain of 0 dB. A negative phase shift implies that a negative feedback loop acts as positive feedback loop and hence making the loop unstable. In this design the capacitor introduces a dominant pole, which allows having a phase margin of 56°.
Layout of the op amp is shown in Fig. 3.15. Figure 3.16 shows the transfer characteristics obtained from DC sweep analysis. The input offset voltage is approximately 16.8 µV. Figure 3.17 shows the transient analysis of operational amplifier. Figure 3.18 shows the frequency response characteristics. The DC gain of the amplifier is 78 dB. The unity gain bandwidth of the amplifier obtained is approximately 9.5 MHz. From the step response shown in the Fig. 3.19 the slew rate of the op amp is 19.95 V/µS. The specifications of the conventional and floating gate input op amps designed are summarized in Table 3.1.

Table 3.1: Specifications of the designed op amps.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Op amp without FG MOSFET at input</th>
<th>Op amp with FGMOS at input</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 dB Gain</td>
<td>78 dB</td>
<td>78 dB</td>
</tr>
<tr>
<td>3 dB BW</td>
<td>1.1 kHz</td>
<td>1.4 kHz</td>
</tr>
<tr>
<td>GBW</td>
<td>12 MHz</td>
<td>9.5 MHz</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>46 V/µs</td>
<td>19.95 V/µS</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>77 °</td>
<td>56 °</td>
</tr>
<tr>
<td>Input offset</td>
<td>1.8 µV</td>
<td>16.8 µV</td>
</tr>
</tbody>
</table>

3.2 Compensation of Two-Stage Op Amp

An important part of an amplifier design is to ensure that the gain of the amplifier is less than unity at the frequency where phase shift around the loop is zero. To achieve this, one of the simplest ways is to give the op amp a dominant pole. Figure 3.20 shows a typical variation of the gain and phase versus frequency which exhibits the gain roll-off after the first dominant pole $p_1$. After the second pole $p_2$, the amplifier becomes unstable or oscillatory since gain becomes greater than unity. A pole-splitting capacitor which is also called miller compensation capacitor is used to push $p_1$ to the left and $p_2$ to the right.
Figure 3.15: Layout of operational amplifier design of circuit of Fig. 3.12.
Figure 3.16: Post layout transfer characteristics of the circuit of Fig. 3.12.

DC input offset voltage = 16.8 µV

Figure 3.17: Post layout simulated response of the CMOS amplifier circuit of Fig. 3.12.
Figure 3.18: Post layout (Fig. 3.15) simulated amplitude and phase versus frequency response characteristics. Note: The 3 dB gain and phase margin are 78 dB and 56°.

Figure 3.19: Post layout (Fig. 3.15) simulated slew rate characteristics of the amplifier circuit of Fig. 3.12.
(Fig. 3.20(b)). Figure 3.21 (b) shows the two-port network equivalent small signal model of the circuit of Figs. 3.3 and 3.12. $V_{id}$ is the differential mode input voltage, $G_{m1}$ is the gain of differential stage equal to $g_{m1}$ and $g_{m2}$, and $G_{m2}$ is the gain of the second stage equal to $g_{m6}$. $R_2$ is the output resistance of second stage equal to $r_{o6} || r_{o7}$. $R_Z$ is the zero nullifying resistance, $C_C$ is the compensation capacitance, $C_2$ is the load capacitance and $R_1$ is the output resistance of first stage equal to $r_{o2} || r_{o4}$. The mid-frequency gain of the op amp circuits shown in of Figs. 3.3 and 3.12 is given by,

$$a_v = \frac{g_{m1}g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds7} + g_{ds6})} \quad (3.13)$$

where

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{I_D} \cong \sqrt{(2\mu_0C_{ox}W/L)|I_D|} \quad (3.14)$$

$$g_{ds} = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_{I_D} \cong I_D\lambda \quad (3.15)$$

in which $\mu_0$ is the channel surface mobility, $C_{ox}$ is the capacitance per unit area of the gate oxide, $W$ and $L$ are the effective channel length and width respectively, $\lambda$ is the channel length modulation parameter of the transistor. $I_D$ represents the quiescent current and is provided by M8, M10 and M5 transistors.

Due to the low transconductance of MOS transistors, the transistor M11 shown in Figs. 3.3 and 3.12 is needed to provide a nullifying resistance to reduce the effects of the right hand plane zero in the transfer function, and in fact, can be used to improve the
Figure 3.20: Effect of pole-splitting capacitor on the gain and phase of an op amp.

frequency response of the amplifier. The small signal equivalent circuit in Fig. 3.21 has two poles and a zero, whose magnitudes are [Ref. 30, pp.644-650],

\[
\omega_{p1} = \frac{1}{G_m R_C R_1}
\]

(3.16)

\[
\omega_{p2} = \frac{G_m C}{C_1 C_2 + C_C (C_1 + C_2)} \approx \frac{G_m}{C_1 + C_2}
\]

(3.17)

and

\[
\omega_z = \frac{1}{(1/G_m - R_z C_C)}
\]

(3.18)

By choosing \(R_z\) to be equal to the inverse of the transconductance of the second stage, the frequency response of the amplifier can be further improved.
Figure 3.21: Two-port network equivalent small signal model of a two-stage op amp configuration of Figs. 3.3 and 3.12 with an equivalent zero nulling resistance ($R_Z$).
CHAPTER 4. $I_{PS}$ BASED TEST METHOD AND FAULT COVERAGE

In analog circuits, the power supply current is a function of input signal, state of the circuit (faulty or faulty free) and value of the parameters of the circuit. The presence of fault in the circuit causes some degree of change in currents in some branches. Those changes in branch currents will result in a more or less significant change in the power supply current [12]. This change in supply current is used to detect faults in a CMOS analog circuit. The test methodology based on the observation of current on the supply rails allows a good coverage of physical defects such as gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetected by conventional logic tests [13]. The major advantage of current based testing is that it does not require propagation of a fault effect to be observed at the output; it requires only existing fault model and then measuring the current from the power supply.

This chapter focuses on $I_{PS}$ testing procedure. Important physical faults commonly seen in the design of CMOS circuits have also been discussed. It also describes the design and implementation of fault injection transistors used to represent open and short circuit faults.

4.1 Power Supply Current ($I_{PS}$) Testing Procedure

$I_{PS}$ based testing has been used to detect faults in a two stage CMOS op amp and this testing method is extended to verify its validity in detecting faults in a CMOS op amp with floating-gate input transistors. In the present work, the AC ripple in the power supply current $I_{PS}$, passing through $V_{DD}$ under the application of an AC input stimulus is measured to detect injected faults in the CUT. The block diagram of power supply current based testing is shown in Fig. 4.1. A small resistor is used to sense the voltage

46
corresponding to the power supply current as shown in Fig. 4.1. The resistor does not affect the performance of the CUT. Input signal to the CUT should produce a noticeable amount of difference between the power supply current of each faulty case and fault-free case. A periodic pulse is selected as input signal to the CUT. AC ripple in the power supply current passing through \( V_{DD} \) is measured without injected faults with a periodic pulse input. In the present work, the tolerance limit for the magnitude of \( I_{PS} \) with no injected faults is defined as \( \pm 5\% \), such that it will take into account the deviations of significant technology and design parameters. The magnitude of ac ripple in the power supply current, \( I_{PS} \) is determined with every injected fault. If the simulated \( I_{PS} \) value falls out of the tolerance limit the fault is detected. In the present work, as mentioned earlier two operational amplifiers one with out floating gate inputs and one with floating gate inputs are designed. Seven bridging faults are introduced in a two stage CMOS op amp with out floating gate input transistors. To consider more number of faults and also the effect of open faults on the performance of FG input CMOS op amp, two chips are fabricated. One of the chips has twenty two short faults and is called as CUT 2 and the other has a combination of twelve short and open faults called as CUT 3. The op amp with seven bridging faults is called as CUT 1.

### 4.1.1 Physical Defects in CMOS Integrated Circuits

In CMOS technology, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS). These defects create indeterminate logic levels at the defect site [13]. Very large-scale integrated circuits processing defects cause shorts or breaks in one or more of the different conductive levels of the device [34]. We briefly discuss these physical defects that cause an increase in the quiescent current.
4.1.1.1 Bridging Faults

Bridges can be defined as undesired electrical connections between two or more lines in an integrated circuit, resulting from extra conducting material or missing insulating material. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate. Bridge between the outputs of independent logic gates or an inter-gate bridge can also occur. Bridging fault could be between the following nodes 1) drain and source, 2) drain and gate, 3) source and gate, and 4) bulk and gate. Figure 4.2 shows an example of possible drain to source and gate to source bridging faults in an inverter chain in the form of low resistance bridges $R_1$ and $R_2$, respectively. Resistance bridge, $R_3$ is an example of inter-gate bridge. Figure 4.3 shows
examples of gate to source and gate to drain bridges in a NAND gate circuit. Bridging defect cannot be modeled by the stuck-at model approach, since a bridge often does not behave as a permanent stuck node to a logic value [35].

Figure 4.2: Drain-source, gate-source and inter-gate bridging faults in an inverter chain.

Figure 4.3: Bridging defects.
4.1.1.2 Open Faults

Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state. Figure 4.4 shows a 2-input NAND with open circuit defects. Node \( V_N \) is in the floating node-state caused due to an open interconnect. For an open defect, a floating gate may assume a voltage because of parasitic capacitances and cause the transistor to be partially conducting [35]. Hence, a single floating gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [36]. In Fig. 4.4, when the node voltage \( (V_N) \), reaches a steady state value, then the output voltage correspondingly exhibits a logically stuck behavior and this output value can be weak or strong logic voltage. Open faults, however, may decrease or may cause only a small rise in \( I_{PS} \) current. An open source or open drain terminal in a transistor may also cause additional power-bus current for certain input states. Another open fault shown in Fig. 4.4 is an open FET \( (M_2) \).

4.1.1.3 Fault Models, Simulation and Detection

Research results claim that 80-90% of observed analog faults are of shorts or opens in diodes, transistors, resistors and capacitors [37]. It is known that when 100% of these faults are detectable, the majority of parametric faults depending on the deviation value of the parametric faults can also be detected [38]. As parametric faults are concerned, a tolerance band of \( \pm 5\% \) is used. This implies that if the values of parameters to be observed in the testing process appropriate to particular faults are within the tolerance band, these faults will be considered as tolerable and cannot be detected.

The primary reason for a fault is a defect in the integrated circuit. A manufacturing defect causes unacceptable discrepancy between its expected performance
Figure 4.4: Floating input and open MOSFET open circuit defects.

at circuit design and actual IC performance after physical realization [36]. A defect may be any spot of missing or extra material that may occur in any integrated circuit layer.

Bridging faults have been induced in the amplifier at various conducting levels using a fault injection transistor (FIT), discussed further ahead, which cause abnormal deviation of the supply current from nominal value. The faults are injected one at a time.

4.1.1.4 Fault Injection Transistor

The faults under consideration are gate-drain shorts, broken wires, floating-gates, drain-source shorts, compensation capacitor short and short circuit between different nodes. In analog CMOS circuits, the faults simulating possible manufacturing defects have been introduced using the fault injection transistors [39]. Activating the fault
injection transistor activates the fault. The use of a fault injection transistor for the fault simulation prevents permanent damage to the operational amplifier by introduction of a physical metal short. This enables the operation of the operational amplifier without any performance degradation in the normal mode. Figure 4.5 (a) shows the fault injection transistor. To create an internal short fault, the fault injection transistor ($M_E$) is connected to opposite potentials. When the gate of fault injection transistor is connected to $V_{DD}$, a low resistance path is created between its drain and source and when connected to $V_{SS}$ a high resistance path is established which represents open circuit. Figure 4.5 (b) shows use of a FIT in simulating a short in the driver of an inverter.

In the Fig. 4.6, internal bridging faults created in the CMOS amplifier between the drain and source nodes using the fault injection transistors are shown. In this work, seven bridging faults *viz.* $M_{10}$ drain-source short (defect 1-M10DSS), $M_5$ gate-drain short (defect 2-M5GDS), $M_5$ drain-source short (defect 3-M5DSS), $M_{11}$ drain-source short (defect 4-M11DSS), $M_4$ gate-drain short (defect 5-CCS), compensation capacitor short (defect 6-M6GDS), $M_7$ gate-drain short (defect 7-M7GDS) have been introduced in the CUT 1.

![Figure 4.5 (a): n-MOS Fault injection transistor (FIT) used in the layout.](image)

Figure 4.5 (a): n-MOS Fault injection transistor (FIT) used in the layout.
Figure 4.5 (b): Fault injection transistor between drain and source nodes of a CMOS inverter.

From the layout of CUT 1 shown in Fig. 4.7, the area of the operational amplifier is $540 \times 186 \ \mu m^2$. The n-MOS fault injection transistor ($M_E$) designed has a maximum aspect ratio ($W/L$) of 41.6/3.2 and the minimum $W/L$ ratio used is 6.4/6.4. The fault injection transistors are activated externally using ERROR signal $V_E$, which is applied to the gate of the fault injection transistor used to represent short or open defect in the operational amplifier circuit.

As the total number of faults introduced in CUT 2 and CUT 3 are more, the presence of short fault between two nodes is represented as $S_{a,b}$ where $a$ and $b$ are the corresponding node numbers. The open fault (broken wire) is represented as $O_a$, where $a$ represents the node number. Figure 4.8 shows floating gate input CMOS op amp with
node numbers. Figures 4.9 and 4.10 show the layouts with fault injection transistors corresponding to CUT 2 and CUT 3, respectively. The fault injection transistors used to represent short faults are with aspect ratios 41.6/3.2, 19.2/3.2 and 6.4/6.4. Open faults are introduced using minimum size transistors with aspect ratio 6.4/1.6 which offer a very high resistance when $V_{SS}$ to is given to their gates. Tables 4.1 and 4.2 show fault numbers relating node or transistor numbers for CUT 2 and CUT 3, respectively.

4.2 Fault Coverage

This section discusses the fault coverage achieved by the power supply current based test approach on the theoretical results obtained from post-layout PSPICE (Cadence Pspice A/D Simulator, V.10) simulations of the two-stage CMOS operational amplifier with and without floating gate inputs, and the observed experimental results. SPICE level 3 MOS model parameters are used in simulation [23], which are summarized in Appendix A. As mentioned earlier three chips were fabricated; one is op amp without floating-gate input transistors called as CUT 1 (Fig. 4.7) and the other two chips are CMOS floating gate input transistor op amps with short faults (Fig. 4.9) and combination of open and short faults (Fig. 4.10), called as CUT 2 and CUT 3, respectively. The chip of CUT 1 was designed using L-EDIT, V.8.3 in standard 1.5 $\mu$m n-well CMOS technology. The other two chips were designed using L-EDIT, V.9.10 in standard 1.5 $\mu$m n-well CMOS technology. The CMOS amplifier designs were put in 2.25 mm $\times$ 2.25 mm size, 40-pin pad frame for fabrication and testing and corresponding padframe layouts are shown in Figs. 4.11(a), (b) and (c).
Figure 4.6: Injected faults using FITs for circuit of Fig. 3.3.
Figure 4.7: Layout of a two-stage CMOS amplifier circuit of Fig. 4.6 showing the defects induced in the CUT using fault injection transistors.
Figure 4.8: A two stage floating gate input CMOS op amp showing node numbers.
Figure 4.9: Layout of two stage CMOS amplifier with FG input transistors showing the short faults induced using FITs (CUT 2).
Figure 4.10: Layout of two stage CMOS amplifier with FG input transistors showing the open and short faults induced using FITs (CUT 3).
### Tables 4.1: Fault numbers related to node or transistor numbers for CUT 2.

<table>
<thead>
<tr>
<th>Short Faults</th>
<th>Fault Representation</th>
<th>Transistor or Node Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault 1</td>
<td>$S_{3,8}$</td>
<td>Node 3-8 Short</td>
</tr>
<tr>
<td>Fault 2</td>
<td>$S_{4,1}$</td>
<td>M3 DSS</td>
</tr>
<tr>
<td>Fault 3</td>
<td>$S_{4,9}$</td>
<td>Node 4-9 Short</td>
</tr>
<tr>
<td>Fault 4</td>
<td>$S_{8,9}$</td>
<td>M5 GDS</td>
</tr>
<tr>
<td>Fault 5</td>
<td>$S_{1,3}$</td>
<td>M10 DSS</td>
</tr>
<tr>
<td>Fault 6</td>
<td>$S_{3,11}$</td>
<td>M8 DSS</td>
</tr>
<tr>
<td>Fault 7</td>
<td>$S_{1,8}$</td>
<td>Node 1-8 Short</td>
</tr>
<tr>
<td>Fault 8</td>
<td>$S_{2,8}$</td>
<td>Node 2-8 Short</td>
</tr>
<tr>
<td>Fault 9</td>
<td>$S_{2,11}$</td>
<td>Node 2-11 Short</td>
</tr>
<tr>
<td>Fault 10</td>
<td>$S_{5,11}$</td>
<td>Node 5-11 Short</td>
</tr>
<tr>
<td>Fault 11</td>
<td>$S_{5,8}$</td>
<td>Node 5-8 Short</td>
</tr>
<tr>
<td>Fault 12</td>
<td>$S_{1,7}$</td>
<td>M6 DSS</td>
</tr>
<tr>
<td>Fault 13</td>
<td>$S_{7,10}$</td>
<td>M7 GDS</td>
</tr>
<tr>
<td>Fault 14</td>
<td>$S_{7,2}$</td>
<td>Node 7-2 Short</td>
</tr>
<tr>
<td>Fault 15</td>
<td>$S_{7,8}$</td>
<td>Node 7-8 Short</td>
</tr>
<tr>
<td>Fault 16</td>
<td>$S_{7,11}$</td>
<td>M7 DSS</td>
</tr>
<tr>
<td>Fault 17</td>
<td>$S_{6,11}$</td>
<td>Node 6-11 Short</td>
</tr>
<tr>
<td>Fault 18</td>
<td>$S_{5,6}$</td>
<td>M11 DSS</td>
</tr>
<tr>
<td>Fault 19</td>
<td>$S_{8,11}$</td>
<td>M5 DSS</td>
</tr>
<tr>
<td>Fault 20</td>
<td>$S_{6,8}$</td>
<td>Node 6-8 Short</td>
</tr>
<tr>
<td>Fault 21</td>
<td>$S_{6,9}$</td>
<td>Node 6-8 Short</td>
</tr>
<tr>
<td>Fault 22</td>
<td>$S_{1,5}$</td>
<td>M4 DSS</td>
</tr>
</tbody>
</table>

### Tables 4.2: Fault numbers related to node or transistor numbers for CUT 3.

<table>
<thead>
<tr>
<th>Open and Short Faults</th>
<th>Fault Representation</th>
<th>Transistor or Node Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault 1</td>
<td>$O_{12}$</td>
<td>Node 12 open</td>
</tr>
<tr>
<td>Fault 2</td>
<td>$O_{13}$</td>
<td>Node 13 open</td>
</tr>
<tr>
<td>Fault 3</td>
<td>$O_{3}$</td>
<td>Node 3 open</td>
</tr>
<tr>
<td>Fault 4</td>
<td>$O_{5}$</td>
<td>Node 7 open</td>
</tr>
<tr>
<td>Fault 5</td>
<td>$O_{7}$</td>
<td>Node 5 open</td>
</tr>
<tr>
<td>Fault 6</td>
<td>$S_{8,11}$</td>
<td>M5 GSS</td>
</tr>
<tr>
<td>Fault 7</td>
<td>$S_{10,11}$</td>
<td>M8 GSS</td>
</tr>
<tr>
<td>Fault 8</td>
<td>$S_{2,1}$</td>
<td>M4 GSS</td>
</tr>
<tr>
<td>Fault 9</td>
<td>$S_{3,1}$</td>
<td>M10 DSS</td>
</tr>
<tr>
<td>Fault 10</td>
<td>$S_{7,1}$</td>
<td>M6 DSS</td>
</tr>
<tr>
<td>Fault 11</td>
<td>$S_{6,11}$</td>
<td>Node 6-7 Short</td>
</tr>
<tr>
<td>Fault 12</td>
<td>$S_{7,11}$</td>
<td>M7 DSS</td>
</tr>
</tbody>
</table>
Op amp with fault injection transistors

Op amp with no fault injection transistors

Figure 4.11(a): CMOS chip layout of a two-stage CMOS amplifier without floating gate input transistors within a padframe of 2.25 mm × 2.25 mm size.
Op amp with only short faults injected (CUT 2)

Figure 4.11(b): CMOS chip layout of a two-stage CMOS amplifier with floating gate input transistors and short faults within a padframe of 2.25 mm × 2.25 mm size.
Figure 4.11(c): CMOS chip layout of a two-stage CMOS amplifier with floating gate input transistors and combined open and short faults within a padframe of 2.25 mm × 2.25 mm size.
In the following sections, theoretical results (simulated from PSPICE) and experimentally measured values will be presented and discussed for the three fabricated chips.

4.2.1 Simulated Amplifier Functional Testing Results

Figures 4.12(a), (b) and (c) show the microphotograph of the fabricated chips of Figs. 4.11(a), (b) and (c). Figure 4.13(a) shows the simulated output response of the CUT 1 (op amp without floating gate input transistors) for a sinusoidal input of 100 mV p-p. Figure 4.13(b) shows measured output response of the op amp without floating gate input transistors for a 200 mV p-p sine wave input. As discussed in Chapter 3, the floating gate input CMOS op amp has a 3 dB bandwidth of 1.4 kHz and a 3 dB gain of 78 dB. With the presence of fault injection transistors that represent short faults the op amp’s performance is not degraded. However, with the presence of open faults which are represented by fault injection transistors, the performance of the op amp is degraded. Transient analysis of CUT 3 is shown in Fig. 4.14. The frequency response of the circuit with combination of open and short faults is shown in Fig. 4.15. This figure shows that the 3 dB gain of the op amp is reduced from 78 dB to 38 dB and phase margin is still 56º. The possible reason for this decrease could be the high resistance offered by the fault injection transistors that represent open faults. The input referred offset for an open loop gain of 38 dB is 15 mV. The offset voltage is increased to a very high value with open faults. However, it is not affected by short faults. Figures 4.16 (a-b) show the op amp as unity gain amplifier with floating gate input transistors with only short faults (CUT 2) and combined open and short faults (CUT 3) when measured experimentally.
Figure 4.12(a): Microphotograph of the fabricated chip showing the CUT 1 (CMOS amplifier).

Figure 4.12(b): Microphotograph of the fabricated chip showing the CUT 2 (CMOS amplifier with floating gate input transistors and short faults).
Figure 4.12(c): Microphotograph of the fabricated chip showing the CUT 3 (MOS amplifier with floating gate input transistors and combined open and short faults).
Figure 4.13(a): Output of the amplifier (CUT 1) for a sinusoidal input voltage of 100 mV p-p.

Figure 4.13(b): Output response of the amplifier (CUT 1) for an input sinusoidal p-p of 200 mV.
Figure 4.14: Post layout transient response of the CUT 3.

Figure 4.15: Post layout frequency response of CUT 3.
Figure 4.16(a): Operational amplifier as unity gain follower for CUT 2.

Figure 4.16(b): Operational amplifier as unity gain follower for CUT 3.
4.2.2 Simulated and Experimental $I_{PS}$ Testing Results

As mentioned in beginning of this chapter, seven short faults were introduced in CUT 1, twenty two short faults were introduced in the CUT 2 and a combination of five open faults and seven short faults were introduced in CUT 3. A 5 kHz 4V peak-to-peak input pulse is applied to CUT 1 and a 1 kHz 4V peak-to-peak to CUT 2 and CUT 3 in the power supply current [$I_{PS}$] based testing. This input stimulus shows significant difference in the power supply current between each of the faulty case and fault-free case. The voltage, $V_R$ is simulated and measured experimentally across a 100 $\Omega$ resistor between $V_{DD}$ and CUT.

Figure 4.17 shows the simulated $I_{PS}$ value for the no fault case and all the seven short faults activated one at a time for CUT 1. From the Fig. 4.17 ac ripple for no fault case is 74 $\mu$A and for Faults 4 and 6 it is 74 $\mu$A. Since the ac ripple of $I_{PS}$ fall within the tolerance range these two faults are not detected. Figures 4.18(i) – (vi) show experimentally measured voltage corresponding to $I_{PS}$ for no fault and faulty cases, where Channel 1 is the ac input stimulus applied to the CUT 1 and circled value shows the output ac ripple measured using Channel 2. Table 4.3 summarizes the simulated and measured results for the CMOS amplifier circuit of Fig. 4.6 (CUT 1) obtained from this testing method. Table 4.3 shows that the SPICE simulated results are in close agreement with the corresponding experimental results. From the simulated results shown in the Table 4.3, Fault 1 – DSS, Fault 2 – GDS, Fault 3 – DSS, Faults 5 – CCS, and Fault 7 – GDS resulted in a large change in $I_{PS}$. On the other hand, Fault 4 – DSS and Fault 6 – GDS produced $I_{PS}$ equal to that of the no fault case. Hence except Fault 4 and 6 all other injected faults have been detected in CUT 1.
Figure 4.17: Post layout magnitude of $I_{PS}$ for no fault and seven injected short faults one at a time for CUT 1.

Table 4.3: SPICE simulated and experimental results for CUT 1.

<table>
<thead>
<tr>
<th>Fault Number</th>
<th>$I_{PS}$ in µA (Simulated)</th>
<th>$I_{PS}$ in µA (Experimental)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No fault</td>
<td>74</td>
<td>74</td>
</tr>
<tr>
<td>Fault 1</td>
<td>804</td>
<td>830</td>
</tr>
<tr>
<td>Fault 2</td>
<td>95</td>
<td>130</td>
</tr>
<tr>
<td>Fault 3</td>
<td>93</td>
<td>120</td>
</tr>
<tr>
<td>Fault 4</td>
<td>74</td>
<td>74</td>
</tr>
<tr>
<td>Fault 5</td>
<td>170</td>
<td>-</td>
</tr>
<tr>
<td>Fault 6</td>
<td>73</td>
<td>74</td>
</tr>
<tr>
<td>Fault 7</td>
<td>156</td>
<td>268</td>
</tr>
</tbody>
</table>
Figure 4.18 (i): $I_{PS}$ when No Fault, Faults 4 and 6 are injected one at a time for CUT1.

(ii) $I_{PS}$ when Fault 1 is injected for CUT1.
(iii) $I_{PS}$ when Fault 2 is injected for CUT1.

(iv) $I_{PS}$ when Fault 3 is injected for CUT1.
(v) $I_{PS}$ when Fault 5 is injected for CUT1.

(vi) $I_{PS}$ when Fault 7 is injected for CUT1.
Figure 4.19(a) and (b) show the simulated $I_{PS}$ values for the fault-free and faulty cases, faults activated one at a time for CUT 2. The figure shows that ac ripple for no fault case is $153 \, \mu A$ and a $\pm 5\%$ tolerance range gives maximum and minimum $I_{PS}$ limits as $145 \, \mu A$ and $161 \, \mu A$. Figure 4.20(i)-(iv) shows measured voltage corresponding to supply current when faults activated one at a time and no fault is activated, where Channel 1 is the ac input stimulus applied to the CUT 2 and circled value shows the output ac ripple measured using Channel 2. The simulated and experimental results using $I_{PS}$ test method for the CUT 2 with short faults are tabulated in Table 4.4. From the SPICE simulations, it can be observed that value of $I_{PS}$ for the injected faults $S_{7,2}$, $S_{7,11}$, $S_{5,6}$ and $S_{8,11}$ fall within the tolerance range and are not detected. $I_{PS}$ value for $S_{4,1}$ activated is $137 \, \mu A$ which is very close to lower tolerance limit is also considered as not detected. The simulated values of $I_{PS}$ for $S_{1,3}$ and $S_{3,11}$ show a large variation from fault free value but the measured $I_{PS}$ for these faults was not as large as shown by SPICE. The fault $S_{6,9}$ shows decrease in measured $I_{PS}$ where as the fault $S_{1,5}$ shows an increase. However, measured $I_{PS}$ for these faults was far away from the tolerance range, and these faults are detected. Out of the twenty two injected short faults except five faults all of them have been detected using $I_{PS}$ based method for a FG input CMOS op amp with only short faults.
Figure 4.19: Post layout magnitude of $I_{ps}$ for short faults (a) No fault through Fault 4 (b) Fault 5 through Fault 10
Figure 4.19: Post layout magnitude of $I_{PS}$ for short faults (c) Fault 11 through 16 and (d) Fault 17 through Fault 22, one at a time for CUT 2.
Table 4.4: SPICE simulated and experimental results for CUT 2.

<table>
<thead>
<tr>
<th>Short Faults</th>
<th>( I_{PS} ) (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SPICE</td>
</tr>
<tr>
<td>No fault</td>
<td>153</td>
</tr>
<tr>
<td>( S_{3,8} )</td>
<td>190</td>
</tr>
<tr>
<td>( S_{4,1} )</td>
<td>137</td>
</tr>
<tr>
<td>( S_{4,9} )</td>
<td>88</td>
</tr>
<tr>
<td>( S_{8,9} )</td>
<td>90</td>
</tr>
<tr>
<td>( S_{1,3} )</td>
<td>670</td>
</tr>
<tr>
<td>( S_{3,11} )</td>
<td>940</td>
</tr>
<tr>
<td>( S_{1,8} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{2,8} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{2,11} )</td>
<td>20</td>
</tr>
<tr>
<td>( S_{5,11} )</td>
<td>71</td>
</tr>
<tr>
<td>( S_{5,8} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{1,7} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{7,10} )</td>
<td>206</td>
</tr>
<tr>
<td>( S_{7,2} )</td>
<td>153</td>
</tr>
<tr>
<td>( S_{7,8} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{7,11} )</td>
<td>152</td>
</tr>
<tr>
<td>( S_{6,11} )</td>
<td>74</td>
</tr>
<tr>
<td>( S_{5,6} )</td>
<td>152</td>
</tr>
<tr>
<td>( S_{5,11} )</td>
<td>136</td>
</tr>
<tr>
<td>( S_{6,8} )</td>
<td>0</td>
</tr>
<tr>
<td>( S_{6,9} )</td>
<td>298</td>
</tr>
<tr>
<td>( S_{1,5} )</td>
<td>19</td>
</tr>
</tbody>
</table>
Figure 4.20 (i): $I_{PS}$ when No Fault is injected for CUT 2.

(ii) $I_{PS}$ when Fault 1 is injected for CUT 2.
(iii) $I_{PS}$ when Faults 7, 8, 11, 12, 14 and 19 are injected for CUT 2 one at a time.

(iv) $I_{PS}$ when Faults 14, 16, 18 and 19 are injected one at a time for CUT 2.
Figure 21 shows the simulated $I_{PS}$ value for the no fault case and different open and short faults activated one at a time. From the Fig. 21 ac ripple for no fault case is 120 $\mu$A. A ± 5% tolerance results a max and min $I_{PS}$ of 126 $\mu$A and 114 $\mu$A, respectively. Figure 4.22(i)-(vi) shows measured voltage corresponding to supply current when faults activated one at a time and no fault is activated, where Channel 1 shows the applied ac input stimulus for CUT 3 and circled value shows the output ac ripple measured using Channel 2. The SPICE simulated and experimental results for no fault and faulty cases of CUT are shown in Table 4.5. For (Open Fault 1) $O_{12}$ the simulated $I_{PS}$ value is same as the no fault and for the other open faults the $I_{PS}$ is stuck at a constant value i.e., did not show any ripple and hence considered as zero $I_{PS}$ and is detected from simulations. These faults also did not show any voltage corresponding to $I_{PS}$ when measured experimentally. Hence, these faults are detected experimentally also. Experimental $I_{PS}$ value for $O_{12}$ showed a considerable deviation from fault free case and hence can be said as detected experimentally. $I_{PS}$ for short faults $S_6$ and $S_7$ is 105 $\mu$A and 737 $\mu$A. Since the ac ripple falls out of the tolerance range these two faults are detected. Faults $O_5$ and $O_7$ resulted in insignificant $I_{PS}$ when measured experimentally. Therefore, it can be said that all the injected open faults were detected by this method. From SPICE and experimental results shown in Table 4.5, faults $S_{9,11}, S_{10,11}$ and $S_{6,11}$ did not show much deviation from the fault free case and were not detectable with $I_{PS}$ test method. For the combined open and short faults case, $I_{PS}$ test method showed negligible $I_{PS}$ for all injected open faults except for one fault where it showed a considerable deviation of $I_{PS}$ from the fault free case. Three of the injected short faults did not show much deviation from the fault free case.
Figure 4.21: Post layout magnitude of $I_{PS}$ for (a) No fault and Fault 1 through Fault 5 (Open Faults) (b) Fault 6 through Fault 12 (Short Faults).
Table 4.5: SPICE simulated and experimental results for CUT 3.

<table>
<thead>
<tr>
<th>Open Short Faults comb.</th>
<th>$I_{PS}$ (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SPICE</td>
</tr>
<tr>
<td>No fault</td>
<td>120</td>
</tr>
<tr>
<td>$O_{12}$</td>
<td>120</td>
</tr>
<tr>
<td>$O_{13}$</td>
<td>0</td>
</tr>
<tr>
<td>$O_{2}$</td>
<td>0</td>
</tr>
<tr>
<td>$O_{5}$</td>
<td>0</td>
</tr>
<tr>
<td>$O_{7}$</td>
<td>0</td>
</tr>
<tr>
<td>$S_{9,11}$</td>
<td>113</td>
</tr>
<tr>
<td>$S_{10,11}$</td>
<td>113</td>
</tr>
<tr>
<td>$S_{2,1}$</td>
<td>0</td>
</tr>
<tr>
<td>$S_{3,1}$</td>
<td>0</td>
</tr>
<tr>
<td>$S_{7,1}$</td>
<td>0</td>
</tr>
<tr>
<td>$S_{6,11}$</td>
<td>105</td>
</tr>
<tr>
<td>$S_{7,11}$</td>
<td>737</td>
</tr>
</tbody>
</table>
Figure 4.22 (i): $I_{PS}$ when No Faults are injected for CUT 3.

(ii) $I_{PS}$ when Open Fault 1 is injected for CUT 3.
(iii) $I_{PS}$ when Open Fault 2 and 3 are injected for CUT 3.

(iv) $I_{PS}$ when Short Fault 1 and 2 are injected one at a time for CUT 3.
(v) $I_{PS}$ when Short Fault 4 is injected for CUT 3.

(vi) $I_{PS}$ when Short Fault 7 is injected for CUT 3.
CHAPTER 5. CONCLUSION

Two CMOS amplifiers are designed: 1) one without floating gate input transistors 2) with floating gate input transistors. The second amplifier circuit was fabricated into two chips one considering only short faults and the other both short and open faults. This is to take into account the performance variation due to the presence of open faults. These CUTs are designed in standard 1.5 µm n-well CMOS technology, with ±2.5 V as supply voltages. A simple methodology for testing the operational amplifier using power supply current measurement based technique is presented. This method is then extended to operational amplifier with FG input transistors. This testing method has improved the fault detection range and can be used to provide additional insights to help identify the fault locations, thus aiding in fault-isolation. The approach is attractive because of its simplicity and robustness. The technique uses a linear resistor to sense the supply voltage corresponding to the supply current. The advantages of the technique are high fault coverage, reduced test time, simple test procedure, and the elimination of a test vector process. This method of testing can be used in combination with other testing methods like oscillation, I_{DDQ} to provide fault confirmation.
REFERENCES

circuit testing for quality assurance in manufacturing: history, current status, and
future trends,” IEEE Trans. on Circuits and Systems II: Analog and Digital Signal

integrated circuits,” IEEE Transactions on Computer Aided Design, vol. 8 no. 2,

integrated circuits: an application of discrimination analysis and hypothesis
testing,” IEEE Transactions on Computer Aided Design, vol. 12, no.1, pp, 102-

of analog integrated circuits,” proc. International Symposium on Circuits and

1990.

581.

using oscillation-test method,” IEEE. Trans. on Computer-Aided Design of


digital-to-analog and analog-to-digital converters,” Proc. 12th Int. Conf. on

1994.


[23] URL: www.mosis.org


APPENDIX A. SPICE LEVEL 3 MOS MODEL PARAMETERS FOR STANDARD N-WELL CMOS TECHNOLOGY [23]

(A) Model Parameters for n-MOS transistors:

.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=1 VTO=0.687 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.5564E-05
+ UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.7822
+ NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01
+ KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7294E-10
+ CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10
+ MJSW=1.00000E-01 PB=9.9000E-01

(B) Model Parameters for p-MOS transistors:

.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=-1 VTO=-0.7574 DELTA=2.9770E+00 LD=1.0540E-08 KP=2.1562E-05
+ UO=191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4099
+ NSUB=6.4040E+15 NFS=5.9090E+11 VMAX=1.6200E+05 ETA=1.4820E-01
+ KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10
+ MJSW=1.5252E-01 PB=7.3574E-01
APPENDIX B. CHIP TESTABILITY

Figure B.1 shows the 2-stage op-amp with out FG input transistors in the 2.25 mm × 2.25 mm padframe. Figure B.2 and Fig. B.3 show the 2-stage op amp with FG input transistors with only short faults and with combined open and short faults in the 2.25 mm × 2.25 mm padframe. It consists of individual sub-modules for testing the chip. The following chips have been fabricated.

<table>
<thead>
<tr>
<th>CHIP No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T4BH-AR</td>
<td>Op-amp with conventional MOS input transistors (CUT 1)</td>
</tr>
<tr>
<td>T4CT-AH 71993</td>
<td>Op-amp with FG MOS transistors at input stage with only short faults (CUT 2)</td>
</tr>
<tr>
<td>T5IL-BL</td>
<td>Op-amp with FG MOS transistors at input stage with combined open and short faults (CUT 3)</td>
</tr>
</tbody>
</table>

(B.1) Inverter module testing:

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Input</td>
</tr>
<tr>
<td>14</td>
<td>Output</td>
</tr>
</tbody>
</table>

DC test was performed on the independent inverter module to test if the chip did not have fabrication problems. Logic ‘0’ is applied at the input pin #16 and output (logic ‘1’) is observed on the pin #14. Logic ‘1’ is applied at the input pin #13 and output (logic ‘0’) is observed on pin #14.

(B.1.1) Operational amplifier module and functional testing

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>Negative op amp input ((V^-))</td>
</tr>
<tr>
<td>37</td>
<td>Positive op amp input ((V^+))</td>
</tr>
<tr>
<td>2</td>
<td>op amp output ((V_{OUT}))</td>
</tr>
<tr>
<td>4</td>
<td>Biasing Input ((V_{BIAS}))</td>
</tr>
</tbody>
</table>
The op-amp is tested in the unity gain configuration by connecting pin #2 to the negative op-amp input pin #36 and giving a 10 mV sine wave to the positive input pin #37. The output has been observed at the pin #2. It has also been tested in the comparator mode by supplying a 4 V peak-to-peak sine wave to the positive input pin #37 observing the output at pin #2 while the negative input pin is being grounded.

(B.1.2) Two stage op amp with out FG MOSFETs at input stage’s testability

Table B.1 summarizes the pin numbers and their description to test the two-stage op-amp.

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BICS output ($V_{BICS}$)</td>
<td>21</td>
<td>2nd op amp node ($M_{3G}$)</td>
</tr>
<tr>
<td>2</td>
<td>op-amp output ($V_{OUT}$)</td>
<td>22</td>
<td>2nd op amp node ($M_{10D}$)</td>
</tr>
<tr>
<td>3</td>
<td>Virtual $V_{SS}$ ($V_{V_{SS}}$)</td>
<td>23</td>
<td>2nd op amp negative input ($V^-$)</td>
</tr>
<tr>
<td>4</td>
<td>EXT input $V_{BIAS}$</td>
<td>24</td>
<td>2nd op amp positive input ($V^+$)</td>
</tr>
<tr>
<td>5</td>
<td>$V_{DD}$ (Corner pad)</td>
<td>25</td>
<td>$V_{SS}$ (Corner pad)</td>
</tr>
<tr>
<td>6</td>
<td>$V_{SHRT}$ 7</td>
<td>26</td>
<td>2nd op amp BICS enable ($V_{ENABLE}$)</td>
</tr>
<tr>
<td>7</td>
<td>$V_{SHRT}$ 6</td>
<td>27</td>
<td>2nd op amp BICS output ($V_{BICS}$)</td>
</tr>
<tr>
<td>8</td>
<td>$V_{SHRT}$ 5</td>
<td>28</td>
<td>2nd op amp EXT pin (EXT)</td>
</tr>
<tr>
<td>9</td>
<td>$V_{SHRT}$ 4</td>
<td>29</td>
<td>2nd op amp output ($V_{OUT}$)</td>
</tr>
<tr>
<td>10</td>
<td>$V_{SS}$</td>
<td>30</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>11</td>
<td>$V_{SHRT}$ 3</td>
<td>31</td>
<td>$V_{DDR}$</td>
</tr>
<tr>
<td>12</td>
<td>$V_{SHRT}$ 2</td>
<td>32</td>
<td>Op amp node ($M_{SD}$)</td>
</tr>
<tr>
<td>13</td>
<td>$V_{SHRT}$ 1</td>
<td>33</td>
<td>Op amp EXT pin (EXT)</td>
</tr>
<tr>
<td>14</td>
<td>Output of test inverter ($INV_{OUT}$)</td>
<td>34</td>
<td>Op amp node ($V_{RZCC}$)</td>
</tr>
<tr>
<td>15</td>
<td>$V_{DD}$ (Corner pad)</td>
<td>35</td>
<td>$V_{SS}$ (Corner pad)</td>
</tr>
<tr>
<td>16</td>
<td>Input of test inverter ($INV_{IN}$)</td>
<td>36</td>
<td>Op amp negative input ($V^-$)</td>
</tr>
<tr>
<td>17</td>
<td>2nd op-amp Virtual $V_{SS}$ ($V_{V_{SS}}$)</td>
<td>37</td>
<td>Op amp positive input ($V^+$)</td>
</tr>
<tr>
<td>18</td>
<td>2nd op-amp node ($M_{6G}$)</td>
<td>38</td>
<td>Op amp node ($M_{6G}$)</td>
</tr>
<tr>
<td>19</td>
<td>2nd op-amp node ($V_{RZCC}$)</td>
<td>39</td>
<td>Op amp node ($M_{3G}$)</td>
</tr>
<tr>
<td>20</td>
<td>2nd op-amp node ($M_{SD}$)</td>
<td>40</td>
<td>Op amp BICS Enable ($V_{ENABLE}$)</td>
</tr>
</tbody>
</table>
(B.1.3) Testing the two-stage op-amp in its normal mode

1. Supply voltages of ± 2.5V is given to the power supply pins of the chip (\(V_{DD}=2.5\) V and \(V_{SS}=-2.5\) V).

2. The \(V_{ENABLE}\) pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode.

3. The EXT pin (#33) is connected to the \(V_{SS}\) (-2.5 V) when the BICS is in the normal mode. (\(V_{ENABLE}=1=+2.5\) V) and \(V_{BIAS}\) pin (#4) is connected to \(V_{DD}\) (+2.5 V).

4. The fault injection transistors must be de-activated by giving a ‘low’ voltage (-2.5 V) to the error-signals \(V_{SHRT1}\), \(V_{SHRT2}\) and so on to \(V_{SHRT7}\).

5. The two-stage op-amp is tested by giving sine wave input in the unity gain feedback mode and comparator mode.

6. The output is observed at pin #2 using an oscilloscope.

(B.1.4) Testing of the op amp in \(I_{PS}\) test mode

1. The \(V_{ENABLE}\) pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode while the EXT pin (#33) is connected to the \(V_{SS}\) (-2.5 V) and \(EXT_{in}\) pin (#4) is connected to the \(V_{DD}\) (+2.5 V) to enable the normal operation of the op-amp.

2. Connect a 100 \(\Omega\) resistor between \(V_{DD}\) pin #30 and \(V_{DDR}\) pin #31.

3. Connect op amp in unity gain configuration in test mode.

4. Deactivate all the fault injection transistors by connecting the corresponding pins to \(V_{DD}\).

5. Input signal of 4 V p-p 1 kHz square wave is applied to the negative input of op amp and corresponding to voltage is measured across the 100 \(\Omega\) resistor using oscilloscope by
keeping it in ac mode. From this voltage power supply current is calculated for no fault case.

6. The fault injection transistors of the faults are activated by giving a ‘high’ voltage (+2.5 V) to the error-signals $V_{SHRT1}$-$V_{SHRT7}$.

7. When the error signals are activated, faults are injected into the chip, which manifest supply current much above the tolerance range. This voltage corresponding to this deviation is observed using the oscilloscope. If this current falls out of ±5% tolerance range then fault is detected.

(B.2.1) Operational amplifier module and functional testing

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Negative op amp input ($V^-$)</td>
</tr>
<tr>
<td>13</td>
<td>Positive op amp input ($V^+$)</td>
</tr>
<tr>
<td>39</td>
<td>Op amp output ($V_{OUT}$)</td>
</tr>
<tr>
<td>12</td>
<td>Biasing Input ($V_{BIAS}$)</td>
</tr>
</tbody>
</table>

The op amp is tested in the unity gain configuration by connecting pin #39 to the negative op amp input pin #11 and giving a 1.5 V at 1 kHz sine wave to the positive input pin #13. The output has been observed at the pin #39. $V_{BIAS}$ pin #12 is connected to $V_{DD}$ (+2.5 V).
Padframe Layout for op amp with out FG input transistors:

Op amp with no faults

Op amp with short faults

Test Inverter
(B.2.2) FG input transistor two stage op amp with short faults and Testability

Table B.2 summarizes the pin numbers and their description to test the two stage op amp.

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BICS output ($V_{BICS}$)</td>
<td>21</td>
<td>$V_{SHRT4}$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{SHRT16}$</td>
<td>22</td>
<td>$V_{SHRT5}$</td>
</tr>
<tr>
<td>3</td>
<td>$V_{SHRT17}$</td>
<td>23</td>
<td>$V_{DDR}$</td>
</tr>
<tr>
<td>4</td>
<td>$V_{SHRT18}$</td>
<td>24</td>
<td>$V_{SHRT6}$</td>
</tr>
<tr>
<td>5</td>
<td>$V_{DD}$ (Corner pad)</td>
<td>25</td>
<td>$V_{SS}$ (Corner pad)</td>
</tr>
<tr>
<td>6</td>
<td>$V_{SHRT19}$</td>
<td>26</td>
<td>$V_{SHRT7}$</td>
</tr>
<tr>
<td>7</td>
<td>$V_{SHRT20}$</td>
<td>27</td>
<td>$V_{SHRT8}$</td>
</tr>
<tr>
<td>8</td>
<td>$V_{SHRT21}$</td>
<td>28</td>
<td>$V_{SHRT9}$</td>
</tr>
<tr>
<td>9</td>
<td>$V_{SHRT22}$</td>
<td>29</td>
<td>$V_{SHRT10}$</td>
</tr>
<tr>
<td>10</td>
<td>$V_{SS}$</td>
<td>30</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>11</td>
<td>$V_{NEG}$</td>
<td>31</td>
<td>$V_{EXT}$</td>
</tr>
<tr>
<td>12</td>
<td>$V_{BIAS}$</td>
<td>32</td>
<td>$V_{-V_{SS}}$</td>
</tr>
<tr>
<td>13</td>
<td>$V_{POS}$</td>
<td>33</td>
<td>$V_{SHRT11}$</td>
</tr>
<tr>
<td>14</td>
<td>Output of test inverter ($INV_{OUT}$)</td>
<td>34</td>
<td>$V_{SHRT12}$</td>
</tr>
<tr>
<td>15</td>
<td>$V_{DD}$ (Corner pad)</td>
<td>35</td>
<td>$V_{SS}$ (Corner pad)</td>
</tr>
<tr>
<td>16</td>
<td>Input of test inverter ($INV_{IN}$)</td>
<td>36</td>
<td>$V_{SHRT13}$</td>
</tr>
<tr>
<td>17</td>
<td>$V_{RZ}$</td>
<td>37</td>
<td>$V_{SHRT14}$</td>
</tr>
<tr>
<td>18</td>
<td>$V_{SHRT1}$</td>
<td>38</td>
<td>$V_{SHRT15}$</td>
</tr>
<tr>
<td>19</td>
<td>$V_{SHRT2}$</td>
<td>39</td>
<td>$V_{OUT}$</td>
</tr>
<tr>
<td>20</td>
<td>$V_{SHRT3}$</td>
<td>40</td>
<td>Op amp BICS Enable ($V_{ENABLE}$)</td>
</tr>
</tbody>
</table>

(B.2.3) Testing the two stage op amp in its normal mode

1. Supply voltages of $\pm 2.5V$ is given to the power supply pins of the chip ($V_{DD}$=2.5 V and $V_{SS}$=-2.5 V).
2. The $V_{ENABLE}$ pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode.
3. The EXT pin (#31) is connected to the $V_{SS}$ (-2.5 V) when the BICS is in the normal mode. ($V_{ENABLE}$ = ‘1’ =+2.5 V).
4. The fault injection transistors must be de-activated by giving a ‘low’ voltage (-2.5 V).
5. \( V_{\text{BIAS}} \) pin (#12) is connected to \( V_{\text{DD}} \) (+2.5 V).

6. The two-stage op-amp is tested by giving sine wave input in the unity gain feedback mode.

7. The output is observed at pin #39 using an oscilloscope.

**(B.2.4) Testing of the op amp in \( I_{\text{PS}} \) test mode**

1. The \( V_{\text{ENABLE}} \) pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode while the EXT pin (#33) is connected to the \( V_{\text{SS}} \) (-2.5 V) and \( \text{EXT}_{\text{in}} \) pin (#4) is connected to the \( V_{\text{DD}} \) (+2.5 V) to enable the normal operation of the op-amp.

2. Connect a 100 \( \Omega \) resistor between \( V_{\text{DD}} \) pin #30 and \( V_{\text{DDR}} \) pin #23.

3. Connect op amp in unity gain configuration in test mode.

4. Deactivate all the fault injection transistors by connecting the corresponding pins to \( V_{\text{DD}} \).

5. Input signal of 4 V p-p 1 kHz square wave is applied to the negative input of op amp and corresponding to voltage is measured across the 100 \( \Omega \) resistor using oscilloscope by keeping it in ac mode. From this voltage power supply current is calculated for no fault case.

6. The fault injection transistors of the faults are activated by giving a ‘high’ voltage (+2.5 V) to the error-signals \( V_{\text{SHRT1}}-V_{\text{SHRT2}} \).

7. When the error signals are activated, faults are injected into the chip, which manifest supply current much above the tolerance range. This voltage corresponding to this deviation is observed using the oscilloscope. If this current falls out of ±5% tolerance range then fault is detected.
Padframe Layout for op amp with only short faults and FG input transistors:
(B.3.1) Operational amplifier module and functional testing

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Negative op amp input ($V^-$)</td>
</tr>
<tr>
<td>9</td>
<td>Positive op amp input ($V^+$)</td>
</tr>
<tr>
<td>2</td>
<td>Op amp output ($V_{\text{OUT}}$)</td>
</tr>
<tr>
<td>8</td>
<td>Biasing Input ($V_{\text{BIAS}}$)</td>
</tr>
</tbody>
</table>

The op amp is tested in the unity gain configuration by connecting pin #2 to the negative op amp input pin #7 and giving a 440 mV at 1 kHz sine wave to the positive input pin #9. The output has been observed at the pin #2.

(B.3.2) FG input transistor two stage op amp with combined open and short faults and testability

Table B.3 summarizes the pin numbers and their description to test the two stage op amp.

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
<th>PIN No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BICS output ($V_{\text{BICS}}$)</td>
<td>21</td>
<td>$V_{\text{BIAS}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>2</td>
<td>$V_{\text{OUT}}$</td>
<td>22</td>
<td>$V_{\text{POS}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>3</td>
<td>$V_{\text{SHRT6}}$</td>
<td>23</td>
<td>$V_{\text{DIFF}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>4</td>
<td>$V_{\text{SHRT7}}$</td>
<td>24</td>
<td>$V_{\text{VSS}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>5</td>
<td>$V_{\text{DD}}$ (Corner pad)</td>
<td>25</td>
<td>$V_{\text{SS}}$ (Corner pad)</td>
</tr>
<tr>
<td>6</td>
<td>$V_{\text{OPEN1}}$</td>
<td>26</td>
<td>$V_{\text{BICS}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>7</td>
<td>$V_{\text{NEG}}$</td>
<td>27</td>
<td>$V_{\text{ENABLE}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>8</td>
<td>$V_{\text{BAIS}}$</td>
<td>28</td>
<td>$V_{\text{EXT}}$ (2\textsuperscript{nd} op amp)</td>
</tr>
<tr>
<td>9</td>
<td>$V_{\text{POS}}$</td>
<td>29</td>
<td>$V_{\text{OPN3}}$</td>
</tr>
<tr>
<td>10</td>
<td>$V_{\text{SS}}$</td>
<td>30</td>
<td>$V_{\text{DD}}$</td>
</tr>
<tr>
<td>11</td>
<td>$V_{\text{OPN2}}$</td>
<td>31</td>
<td>$V_{\text{OPN4}}$</td>
</tr>
<tr>
<td>12</td>
<td>$V_{\text{DDR}}$</td>
<td>32</td>
<td>$V_{\text{SHRT3}}$</td>
</tr>
<tr>
<td>13</td>
<td>$V_{\text{SHRT1}}$</td>
<td>33</td>
<td>$V_{\text{SHRT4}}$</td>
</tr>
<tr>
<td>14</td>
<td>Output of test inverter ($V_{\text{OUT}}$)</td>
<td>34</td>
<td>$V_{\text{EXT}}$</td>
</tr>
<tr>
<td>15</td>
<td>$V_{\text{DD}}$ (Corner pad)</td>
<td>35</td>
<td>$V_{\text{SS}}$ (Corner pad)</td>
</tr>
<tr>
<td>16</td>
<td>Input of test inverter ($V_{\text{IN}}$)</td>
<td>36</td>
<td>$V_{\text{VSS}}$</td>
</tr>
<tr>
<td>17</td>
<td>$V_{\text{SHRT2}}$</td>
<td>37</td>
<td>$V_{\text{SHRT5}}$</td>
</tr>
<tr>
<td>18</td>
<td>$V_{\text{OUT}}$ (2\textsuperscript{nd} op amp)</td>
<td>38</td>
<td>$V_{\text{OPN5}}$</td>
</tr>
<tr>
<td>19</td>
<td>$V_{\text{RZ}}$</td>
<td>39</td>
<td>$V_{\text{RZ}}$</td>
</tr>
<tr>
<td>20</td>
<td>$V_{\text{NEG}}$ (2\textsuperscript{nd} op amp)</td>
<td>40</td>
<td>Op amp BICS Enable ($V_{\text{ENABLE}}$)</td>
</tr>
</tbody>
</table>
(B.3.3) Testing the two-stage op-amp in its normal mode

1. Supply voltages of ± 2.5V is given to the power supply pins of the chip (V_{DD}=2.5 V and V_{SS}=-2.5 V).

2. The V\text{ENABLE} pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode.

3. The EXT pin (#34) is connected to the V_{SS} (-2.5 V) when the BICS is in the normal mode. (V\text{ENABLE}= ‘1’ =+2.5 V).

4. The fault injection transistors must be de-activated by giving a ‘low’ voltage (-2.5 V).

5. V\text{BIAS} pin (#8) is connected to V_{DD} (+2.5 V).

6. The two stage op amp is tested by giving sine wave input in the unity gain feedback mode.

7. The output is observed at pin #2 using an oscilloscope.

(B.3.4) Testing of the op-amp in I_{PS} test mode

1. The V\text{ENABLE} pin (#40) is given a ‘high’ voltage (+2.5 V), which makes the BICS to function in the normal mode while the EXT pin (#34) is connected to the V_{SS} (-2.5 V) to enable the normal operation of the op-amp.

2. Connect a 100 Ω resistor between V_{DD} pin #30 and V_{DDR} pin #2

3. Connect op amp in unity gain configuration in test mode.

4. Deactivate all the fault injection transistors by connecting the corresponding pins to V_{DD}.

5. Input signal of 4 V p-p 1 kHz square wave is applied to the negative input of op amp and corresponding to voltage is measured across the 100 Ω resistor using oscilloscope by
keeping it in ac mode. From this voltage power supply current is calculated for no fault case.

6. The fault injection transistors of the faults are activated by giving a ‘high’ voltage (+2.5 V) to the error-signals $V_{SHRT1-V_{SHRT7}}$ and the open-fault is activated by giving a ‘low’ voltage (-2.5 V) to the error-signal $V_{OPN1-V_{OPN5}}$.

7. When the error signals are activated, faults are injected into the chip, which manifest supply current much above the tolerance range. This voltage corresponding to this deviation is observed using the oscilloscope. If this current falls out of ±5% tolerance range then fault is detected.
Padframe Layout for op amp with open and short faults and FG input transistors:

Op amp with open and short faults

Op amp with no faults

Test Inverter
VITA

Vanikumari Pulendra was born on April 20, 1979, in Tirupati, India. She received her Bachelor of Engineering in Electronics and Communications Engineering from Osmania University, Hyderabad, India, in April 2001. She is enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, since August 2002 to attend graduate school. Her research interests include analog and digital integrated circuits design and testing.