

A STUDY OF PHASE NOISE AND JITTER IN SUBMICRON CMOS PHASE-LOCKED LOOP CIRCUITS

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ABSTRACT

Phase-locked loops (PLLs) are widely used in communication systems. With the continuously expanding of market for high speed, portable communication devices, low noise CMOS submicron integrated circuit designs of PLL for different applications are in large demand. In this dissertation, phase noise and jitter properties of PLL and its building blocks are investigated both at the physical and system levels.

At the physical level, hot carrier effect in submicron MOSFETs has been considered. As one of the most dominant noise sources of PLL, the voltage-controlled oscillator (VCO) is considered when investigating the noise degradation induced by the hot carrier effect. Experimental results of jitter degradation due to hot carrier effects are presented for different ring oscillator types VCOs designed in 0.5 μm n-well CMOS technology. An increase in RMS jitter by 25% and 10% decrease in oscillation frequency of VCO can be observed after 4 hours hot carrier stress. The hot carrier induced noise degradation on PLL is also presented based on the performance degradation in VCO. Simulation results show 40% decrease in VCO gain after 4 hours stress and a 23% decrease in damping factor and loop bandwidth. Moreover, degradation on PLL noise performance includes a left shift peak in phase noise and a 17% increase in RMS jitter.

At the system level, noise sources in a PLL system are investigated including the input reference noise, VCO noise and the frequency divider noise. Phase noise prediction method for PLL is developed. Experimental phase noise measurement results on 0.5 μm CMOS PLL systems based on different types of VCOs are in close agreement with the predicted phase noise. Therefore, the phase noise prediction method is verified. On the other hand, a 3 GHz adaptive bandwidth PLL based on LC-VCO is designed in 0.25 μm n-well CMOS technology to

investigate the phase noise and jitter performance by varying the loop parameters. By considering the noise simulation results based on the adaptive bandwidth feature and the quality factor of the on-chip inductor, PLL loop parameters can be carefully chosen at the design phase to achieve an optimal noise performance.

CHAPTER 1

INTRODUCTION

Phase-locked loops (PLLs) are a well established and very widely used circuit technique in modern electronic systems, which are used primarily in communication systems. In essence, PLLs are circuits in which the phase of a local oscillator is maintained close (or locked) to the phase of an external signal. This technique was first developed in the 1930's as a means of implementing a zero intermediate frequency (IF) synchronous receiver. Examples of the many successful applications of PLLs include line synchronization and color sub-carrier recovery in TV receivers, local oscillators and FM or PM demodulators in radio receivers and frequency synthesizers in transceivers (such as mobile phones) and signal generators. The basic operation of a PLL is deceptively simple, however the detailed design of a PLL circuit for a particular application often requires a great deal of understanding of the underlying principles of operation, circuit properties and associated limitations.

Nowadays, with the continuously expanding of market for high speed, portable communication devices, low power and low noise integrated circuit designs of PLL for different applications are in large demand. Among several available technologies, such as bipolar junction transistor (BJT), gallium arsenide (GaAs), complementary metal-oxide-semiconductor (CMOS) and bipolar CMOS (BiCMOS) [1-3], the CMOS technology has played a key role in low power, low noise PLL design. CMOS based PLL designs for different applications are reported in [4-10]. PLL applications in transceiver and receiver in communication systems are presented in [4, 5]; PLL as clock synthesizers in microprocessor applications are shown in [6, 7]; PLL system-on-chip (SoC) applications are discussed in [8, 9]; and PLL in data recovery circuits is reported in [10].

Furthermore, clock signals are required in most of the electrical systems. As clock speed in communications systems pushes into the GHz range, phase noise and jitter, which are key issues in analog designs, are becoming increasingly critical to the performance of digital chips and boards. Timing errors in the clock or oscillator waveforms of high-speed systems can limit the maximum speed of a digital I/O interface, increase the bit error rate of a communications link, or even cap the dynamic range of an A/D converter. Given this trend, designers of high-speed digital equipment are beginning to pay greater attention to timing issues. A typical PLL consists of five fundamental components as shown in Fig. 1.1 [11]. These are a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider. Noise issues have been addressed for each of these components. For example, noise analysis on PFD is shown in [12], jitter and noise studies of ring oscillator are shown in [13-15], and divider noise analysis is shown in [16]. The noise analyses on the whole PLL system from different aspects are reported in [17-23].

The work in this dissertation is mainly focused on the phase noise and jitter analysis in the VCO and in the PLL. With the continuously increased demand for very large scale integrated (VLSI) circuits, feature size of the CMOS transistors continue to decrease. In submicron CMOS, the performance of integrated circuits is influenced due to hot carrier effect. Hot carrier induced device degradation model has been applied in studying the performance of submicron CMOS circuits [24-30]. However, there is no reported work focusing on hot carrier effects on the phase noise and jitter degradation on VCO and PLL. In the presented work, we have studied phase noise and jitter degradation in VCO and in PLL due to hot carrier effect and reported in [31-33]. In another study, we have extended our work in the performance analysis of OFDM systems which are reported in [34-38].

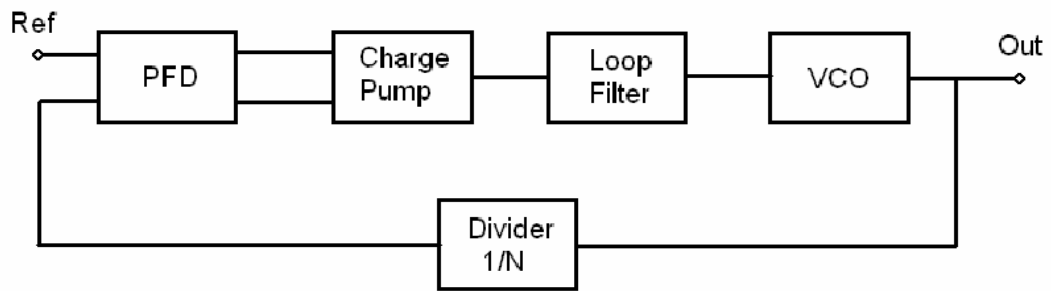


Figure 1.1: A block diagram of PLL.

Moreover, for further understanding of the phase noise and jitter in PLL, an experimental phase noise study which verifies the PLL phase noise prediction method is described in this dissertation. Also phase noise and jitter studies on an adaptive bandwidth PLL are carried out to investigate the noise performance of PLL based on different loop components. Due to some limitation, experimental circuits are fabricated in 0.5 μm CMOS process in this work. However, the results can be extended to deep submicron CMOS technology.

In the following sections, definitions of phase noise and jitter will be given, basic PLL component circuit design will be reviewed, and the physical origin and device degradation model of hot carrier effect will be introduced.

1.1 Jitter and Phase Noise

Clock quality is usually described by jitter or phase noise measurements. Phase noise and jitter are different ways of quantifying the same phenomenon [39, 40]. Jitter is a measurement of the variations in the time domain, and essentially describes how far the signal period has wandered from its ideal value. In another word, jitter is the deviation of a clock's output transitions from their ideal positions. In an ideal clock's output, clock frequency is constant, thus, the spacing between transitions is also constant. However, in practice, the transition spacing may vary from time to time. This uncertainty is known as clock jitter and increases with the measurement interval, ΔT , which is the time difference between the reference and the observed transitions, as shown in Fig. 1.2. And the uncertainty in an earlier transition affects all the following transitions, which is called jitter accumulation. Therefore, the total timing uncertainty after measurement interval, ΔT , is the sum of the uncertainties associated with each transition. There are two common jitter specifications: peak-to-peak jitter and RMS (root mean-squared) jitter. Peak-to-peak jitter characterizes the maximum difference between the measured transitions

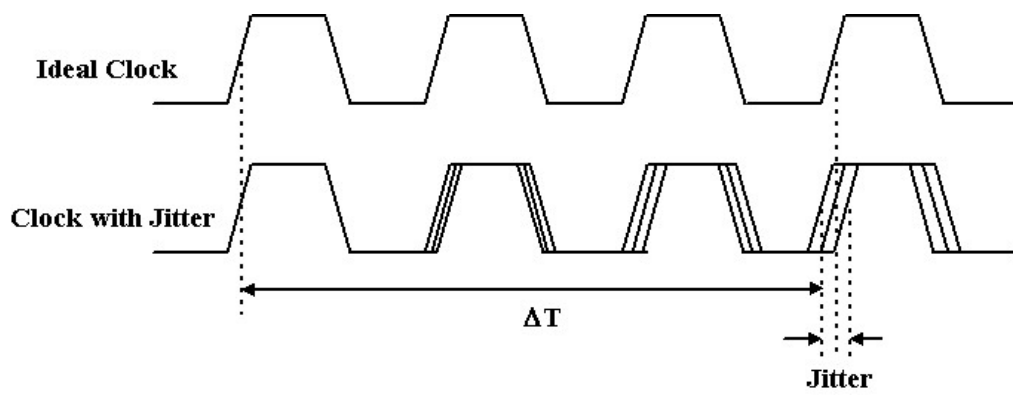


Figure 1.2: Clock jitter increases with the measurement interval, ΔT .

to its ideal position. In most circuits, this value increases with the number of samples taken, theoretically up to a value of infinity. Under these circumstances, it is a not very useful measure. RMS jitter is the value of one standard deviation of the normal distribution. Since this value changes very little as the number of samples increases, it is a more meaningful measurement.

Phase noise is the measure of variations in the frequency domain. Figure 1.3 shows a plot of an oscillator signal exhibiting phase noise. If phase noise wasn't present, the entire power of the oscillator would be focused at the center frequency ω_0 . However, phase noise spreads some of the oscillator's power to adjacent frequencies, which results in sidebands. In Fig 1.3, the sidebands are shown falling off at $\omega_0 + \Delta\omega$. $\Delta\omega$ is the offset from the center frequency. A signal's short-term instabilities are usually characterized in terms of the single sideband noise spectral density. It has units decibels below the carrier per hertz (dBc/Hz) and is defined as [14]

$$L_{total}\{\Delta\omega\} = 10 \log \left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})}{P_{carrier}} \right] \quad (1.1)$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})$ represents the single sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz. This definition includes the effect of both amplitude and phase fluctuations. However, amplitude noise can be practically eliminated by the application of a limiter to the output signal. The phase fluctuation is more important for RF applications. Therefore, in most applications, $L_{total}\{\Delta\omega\}$ is dominated by its phase portion, known as the phase noise, and simply denoted as $L\{\Delta\omega\}$. In Fig. 1.3, phase noise is represented by the ratio of the area of the rectangle with 1-Hz bandwidth at offset $\Delta\omega$ to the total area under the power spectrum curve, approximately the difference in the height of the spectrum at the center ω_0 and at $\omega_0 + \Delta\omega$. The spectrum is the power spectrum of an oscillator with a noisy phase angle.

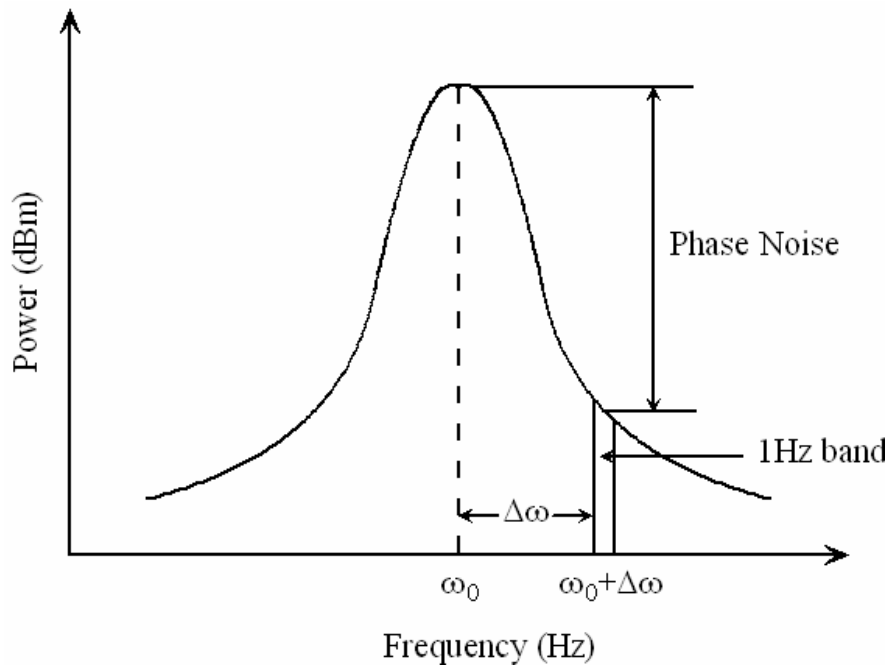


Figure 1.3: Oscillator power spectrum with phase noise at an offset frequency $\Delta\omega$ from the center frequency ω_0 .

The spectrum of these phase-angle fluctuations themselves can also be shown, as in Fig. 1.4. To be clear, the spectrum in Fig. 1.3 is the power spectrum of the oscillator, while the spectrum in Fig. 1.4 is the noisy phase angle term, called the spectral density function of phase noise. For offsets sufficiently far from the carrier, the phase noise in dBc/Hz measured from the power spectrum in Fig. 1.3 is equal to the value of the power spectral density of phase noise in Fig. 1.4. The spectrum in Fig. 1.4 is shown on a log-log scale. In practice, there are regions in the sidebands where the phase can fall at $1/f^3$, $1/f^2$ and $1/f^0$, depending on the noise process involved. The $1/f^2$ region is due to the white, or uncorrelated, fluctuations in the period of the oscillator. The behavior in this region is dominated by the thermal noise in the devices. For lower offset frequencies, the flicker noise of devices generally comes into the picture and the spectrum in this region falls at $1/f^3$. As offset frequency approaches zero, the sidebands grow towards infinity. This is consistent with the phase noise behavior expected in open loop VCOs. In this dissertation, the thermal noise which is of the main concern in a PLL or VCO circuit has been focused for study. Therefore, only the $1/f^2$ region is considered throughout the work.

Phase noise and jitter are very important properties of a PLL. Because PLL is a frequency synchronizer, phase noise or timing jitter on the output of a PLL will dramatically affect the performance of the whole communication system. The presented research will focus on noise issues in PLL circuits.

1.2 Phase-Locked Loop Components and Properties

Five fundamental components of PLL are shown in Fig. 1.1. These are phase/frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and $1/N$ frequency divider. The PLL operates as follows: The phase difference between the reference clock and the output clock (frequency divided by N) is detected by PFD. The output of the PFD, which carries the information of phase difference between two inputs, is transferred as a control

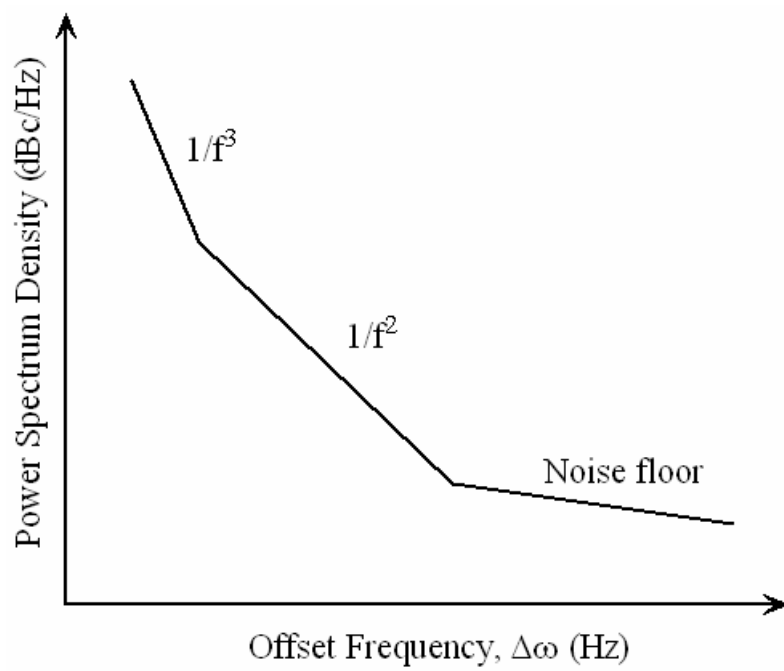


Figure 1.4: Phase noise power spectrum density.

voltage of the VCO by a charge pump and a loop filter. Charge pump is used to charge or discharge the loop filter capacitance, in order to achieve a control voltage which follows the PFD output. The VCO eliminates the phase difference by adjusting the frequency of the output clock with the variation of the control voltage. The $1/N$ divider makes it possible to generate an output clock with a frequency that is exactly N times of the reference clock. N is not necessary to be an integer. When the PLL is settled down or the PLL is locked, the VCO output clock should have the same phase as the reference clock. That is the reason why the circuit is named by phase-locked loop. Each one of the components will be discussed in detail in the following sections.

1.2.1 Phase/Frequency Detector (PFD)

Figure 1.5 shows a simple D-Flip-flop (DFF) based PFD [11]. The output of the PFD depends on both the phase and frequency of inputs (Ref and VCO outputs). This type of phase detector is also termed a sequential phase detector. It compares the leading edges of the reference clock and the divided by N output clock of VCO. There are two output signals from PFD, one is UP and the other one is DN. Figure 1.6 (a) and (b) may help in understanding the principle of the PFD. Two cases are shown for same input frequency and different input frequencies. Consider the case with the same input frequencies depicted in Fig. 1.6 (a). When the reference clock rising edge (phase) is leading the VCO clock (assuming $N=1$ for simplicity), UP will be a sequence of positive pulses, the pulse width is exactly same as the difference of the rising edges of two inputs, while DN will be at low level except some narrow spurs. On the other hand, when the VCO clock is leading, DN will be a sequence of positive pulses with pulse width same as the phase difference, while UP will be at low except some narrow spurs. When both the reference clock and the VCO clock have the same phase, UP and DN will both be at low level except the narrow spurs. In the case in Fig. 1.6 (b), the reference clock rising edge is always leading the VCO clock, therefore, DN is always low.

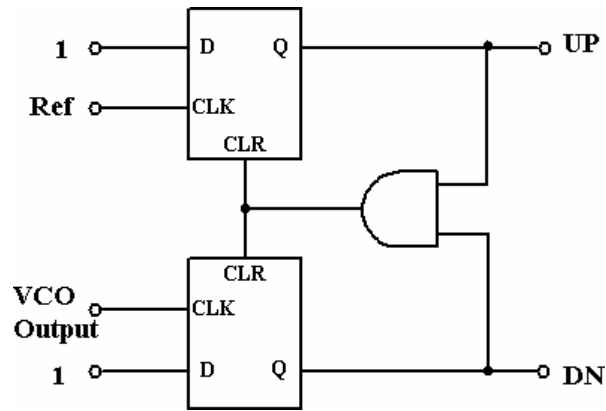
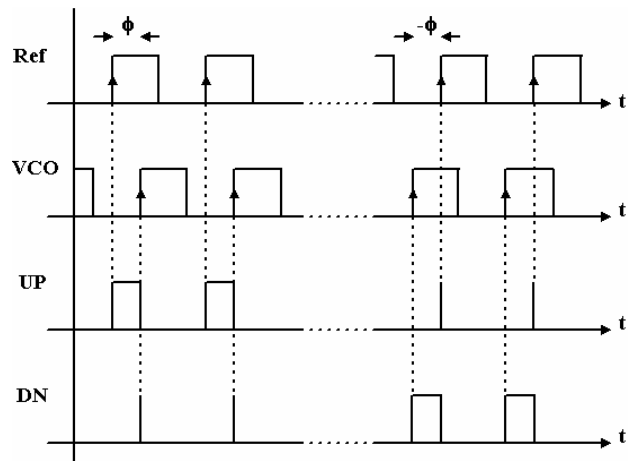
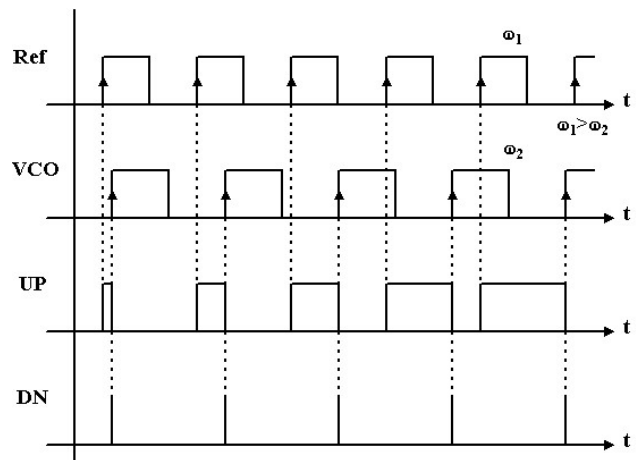


Figure 1.5: A phase/frequency detector (PFD).



(a)



(b)

Figure 1.6: PFD outputs with (a) same frequency inputs, (b) different frequency inputs.

1.2.2 Charge Pump

A charge pump is needed to combine the UP and DN outputs of the PFD into a single output for driving the loop filter. An equivalent diagram of charge pump is shown in Fig. 1.7. CMOS current sources are placed in series with switches S_1 and S_2 . When the PFD output UP signal goes high, S_1 turns on, connecting the charge pump current I_{CH} to the loop filter. This will inject charge into a loop filter capacitor, C_1 , which in turn results in an increase in the output voltage of loop filter, control voltage, to adjust the VCO output frequency. As long as the dynamics of the loop are much slower than the signal, the charge pump can be treated as a continuous time integrator. Usually a zero is introduced by adding a resistor in series with the capacitor to improve the stability of the loop. The details will be discussed in the loop filter section.

1.2.3 Voltage-Controlled Oscillator (VCO)

The input of a VCO is typically a control voltage, V_{CTRL} . Sometimes, current controlled oscillators (CCOs) are used. The output of a VCO is a clock signal, the frequency of which can be adjusted by varying V_{CTRL} . A current starved VCO is shown in Fig. 1.8 [11]. Its operation is similar to the ring oscillator. MOSFETs M2 and M3 operate as an inverter while MOSFETs M1 and M4 operate as current sources, which limit the current available to the inverter, or in other words the inverter is starved for current. MOSFETs M5 and M6 are mirrored in each inverter current source stage. The oscillation is achieved by charging and discharging the equivalent output capacitance in each stage of the VCO. The simplified schematic of one stage of the VCO is shown in Fig. 1.9.

The oscillation frequency of the current starved VCO for n (an odd number ≥ 3) of stages is given by [11]

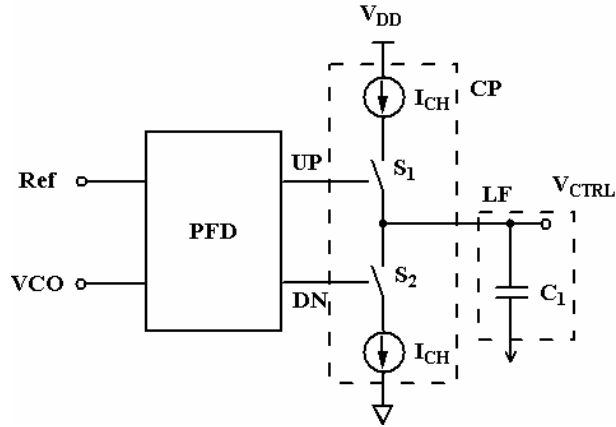


Figure 1.7: An equivalent diagram of a charge pump.

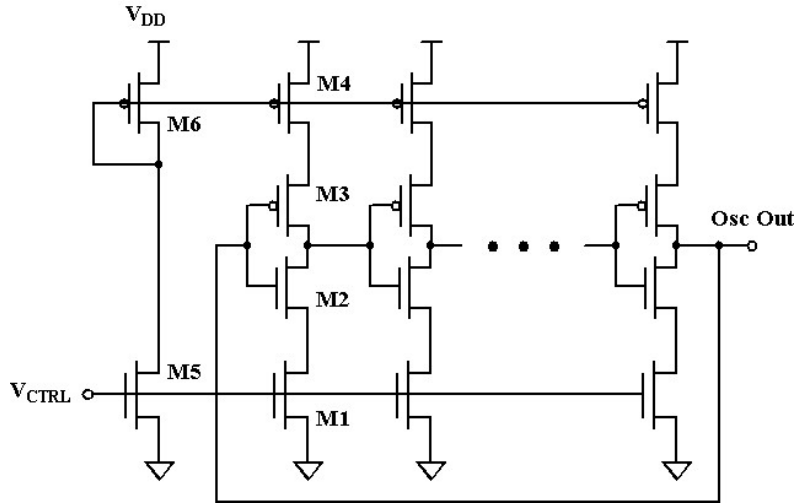


Figure 1.8: A current starved VCO.

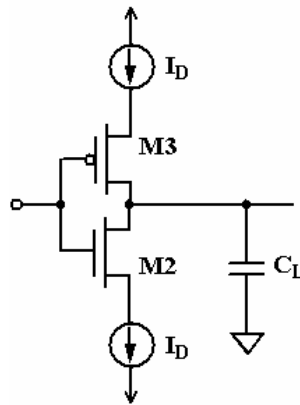


Figure 1.9: A single stage of a current starved VCO with equivalent capacitance.

$$f_o = \frac{1}{n(t_r + t_f)} \approx \frac{I_D}{n \cdot C_L \cdot V_{DD}} \quad (1.2)$$

where t_r and t_f are the rise time and the fall time, respectively, and n is the number of stages. V_{DD} is the power supply voltage. I_D is the biasing current of M2 and M3. The biasing current can be adjusted by varying the control voltage, which in turn adjusts the oscillation frequency.

There are also other types of VCO configurations, such as source coupled differential VCO and LC tank VCO [11].

1.2.4 Loop Filter and Loop Dynamics

The loop filter is very important in a PLL. A passive loop filter is shown in Fig. 1.10. A resistor R is in series with a capacitor C_1 and another capacitor C_2 is in parallel with R and C_1 . C_1 and the charge pump serve as an integrator which can adjust control voltage. R is to improve the stability of the loop. C_2 is used to keep voltage drop on R from causing voltage jumps on the control voltage of the VCO and thus frequency jumps in the VCO output. In general, the value of C_2 is set much lower than one-tenth of the value of C_1 , so that it can be neglected in considering the loop dynamics. The configuration of loop filter is not unique. There are active loop filters in PLL. However, the passive loop filter presented is widely used in PLL design and in PLL noise analysis. The values of components of the loop filter dramatically affect the loop dynamics.

To investigate the loop dynamics of PLL, a phase domain block diagram is more useful, which is shown in Fig. 1.11. $\Phi_{in}(s)$ and $\Phi_{out}(s)$ are the reference input phase and VCO output phase, respectively, $\Phi_e(s)$ is the phase error between $\Phi_{in}(s)$ and $\Phi_{out}(s)$. PFD is characterized as a multiplier and a gain stage with gain K_P . Loop filter has a transfer function of $F(s)$. VCO gain is defined as K_V (rad/s/V), since frequency is the derivation of phase with respect to time, $d\Phi_{out}(t)/dt = K_V V_{ctrl}(t)$, or, $\Phi_{out}(s) = V_{ctrl}(s)K_V / s$ in frequency domain.

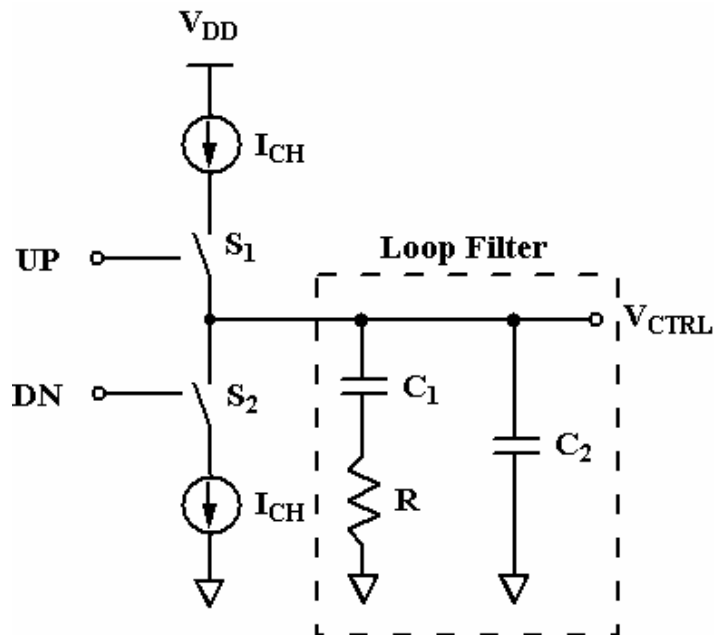


Figure 1.10: A passive loop filter following the charge pump.

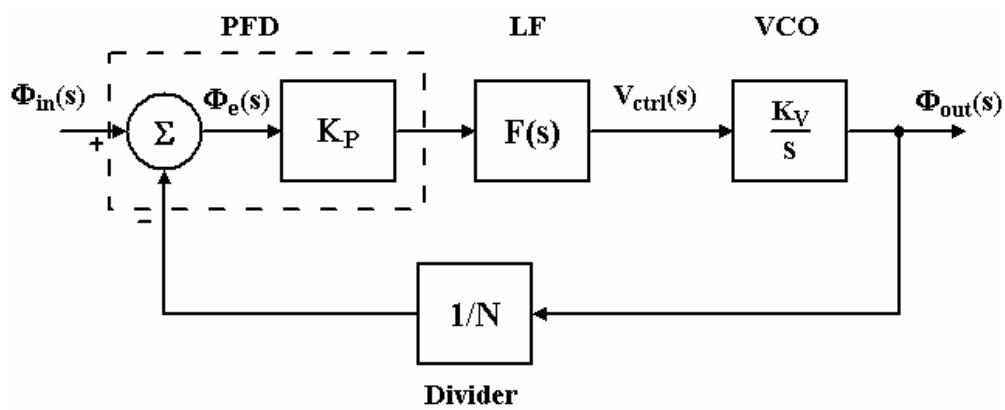


Figure 1.11: A phase domain block diagram of PLL.

The closed-loop response can be carried out by looking into the output phase and input phase relation, which is given by [41]

$$\Phi_{out}(s) = \left\{ \Phi_{in}(s) - \frac{\Phi_{out}(s)}{N} \right\} \cdot K_p \cdot F(s) \cdot \frac{K_v}{s} \quad (1.3)$$

or

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = H(s) = \frac{N \cdot K_p \cdot F(s) \cdot K_v}{N \cdot s + K_p \cdot F(s) \cdot K_v} \quad (1.4)$$

where $H(s)$ is defined as the close loop transfer function of PLL. For the loop filter shown in Fig. 1.10, neglecting C_2 , the loop filter transfer function is given by

$$F(s) = \frac{1 + s\tau}{sC_1} \quad (1.5)$$

where $\tau = R \cdot C_1$, a time constant. $1/\tau$ is the frequency of the zero.

As long as the charge pump switches are much faster than the loop dynamics, the combined PFD/loop filter transfer function is given by

$$K_p \cdot F(s) = \frac{I_{CH}}{2\pi C_1} \cdot \frac{s\tau + 1}{s} \quad (1.6)$$

where I_{CH} is the charge pump output current and $K_p = I_{CH} / 2\pi$. Equations (1.4) and (1.6) lead to the following closed-loop transfer function for the PLL:

$$H(s) = \frac{N \cdot (1 + s\tau)}{1 + s\tau + s^2 / \left(\frac{K_v I_{CH}}{2\pi N C_1} \right)} \quad (1.7)$$

If K_v is defined in Hz/V, we can get

$$H(s) = \frac{N \cdot (1 + s\tau)}{1 + s\tau + s^2 / \left(\frac{K_v I_{CH}}{N C_1} \right)} \quad (1.8)$$

$$H(s) = N \cdot \frac{1 + 2 \cdot \zeta \cdot (s / \omega_n)}{1 + 2 \cdot \zeta \cdot (s / \omega_n) + (s / \omega_n)^2} \quad (1.9)$$

where ζ , defined as the damping factor, is given by [41]

$$\zeta = \frac{1}{2} \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot R^2 \cdot C_1} \quad (1.10)$$

and ω_n , defined as the loop bandwidth (rad/s), is given by

$$\omega_n = \frac{2 \cdot \zeta}{R \cdot C_1} = \sqrt{\frac{K_V I_{CH}}{N C_1}}. \quad (1.11)$$

The loop bandwidth and damping factor characterize the closed-loop response. In general, ω_n determines the cut-off frequency of the response and ζ determines the shape of the characteristic. PLL is critically damped with a damping factor of one and over damped with damping factors greater than one. Note that the closed-loop transfer function has two poles neglecting the capacitance of C_2 . The PLL is therefore called a second order PLL. The frequency response, and step response are shown in Fig. 1.12 and 1.13, respectively, with different damping factors.

1.3 Hot Carrier Induced Device Degradation

As device feature size decreases to sub-micron level, short-channel MOSFETs may experience high lateral electric fields if the drain-source voltage is large. While the average velocity of carriers saturates at high fields, the instantaneous velocity and hence the kinetic energy of the carriers continue to increase, especially as they accelerate towards the drain end. These high energy carriers, known as hot carriers, can cause degradation of device performance by creating interface traps and oxide trapped charges [25]. The hot carrier effect has significantly influenced the small geometry devices and, therefore, it should be taken into consideration for high frequency applications. Hot carrier effects are presented in the following sections.

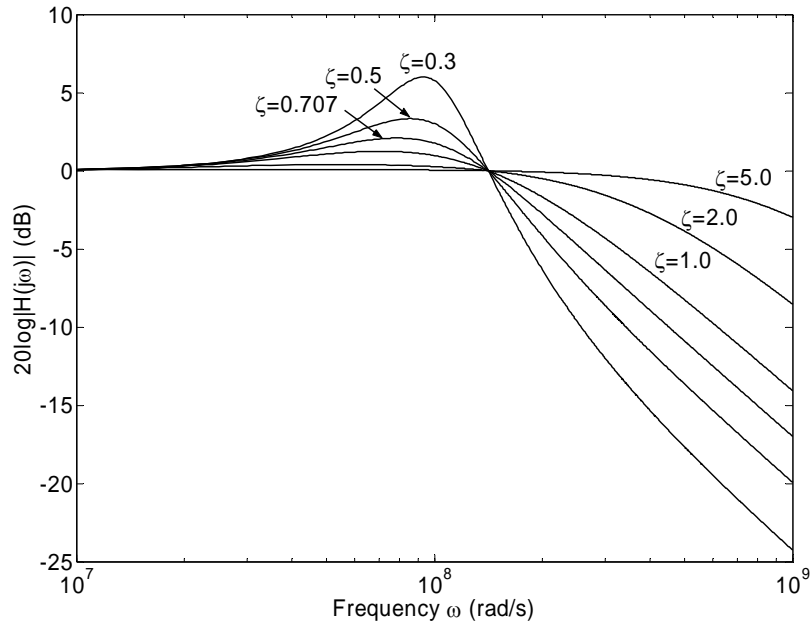


Figure 1.12: Frequency response of PLL with different damping factors.

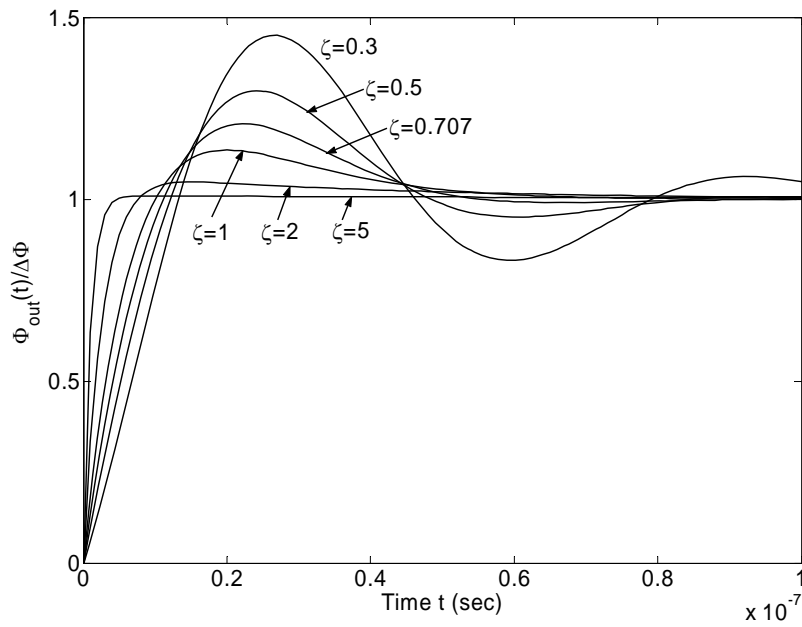


Figure 1.13: Step response of PLL with different damping factors.

1.3.1 A Physical Model for Hot Electron Induced Interface Traps

MOSFET degradation is dominated by the generation of acceptor-type interface traps, which are localized in a narrow band near the drain and reduce local mobile carrier density and mobility. The interface traps responsible for device degradation are generated by hot electrons having energies larger than about 3.7 eV [25]. A possible microscopic mechanism is that a hot electron breaks a silicon-hydrogen bond, shown in Fig 1.14. If the resultant trivalent silicon atom recombines with hydrogen, no interface trap is generated. On the other hand, if the hydrogen atom diffuses away from the interface, a new interface trap is generated. The diffusion process leads to the t^n dependence, where t is the stress time, and the parameter n ranges between 0.5-0.75 [25]. A hot electron breaks the $\equiv Si_s H$ bond to produce S_i^* , trivalent silicon atom, which forms interface traps, and H_i , interstitial hydrogen atom. This process can be described by the following equation



The interface trap density is characterized by parameter N_{it} , which is responsible for the device degradation.

The $\equiv Si_s H$ bonds are formed at the interface during post-metallization anneal. The strength of this bond is about 0.3 eV. This bond energy plus the 3.2 eV $S_i - S_i O_2$ barrier energy is close to 3.7 eV. The difference may be due to data inaccuracies, three-dimensional momentum considerations, or the retarding field in silicon. Moreover, electron energy is not limited to qV_D . It has been argued that electrons in channel are in quasi-thermal equilibrium probably due to electron-electron scattering. More accurately, the hot-electron energy distribution is basically field dependent rather than voltage dependent. Although the break point energy is 3.7 eV, even

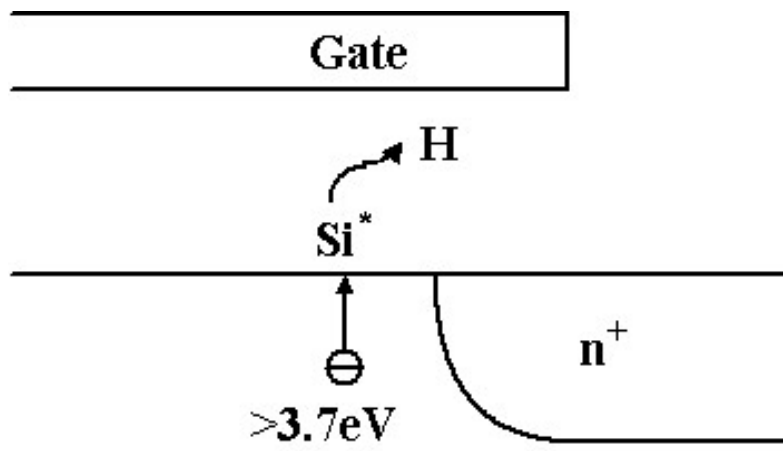


Figure 1.14: A physical model for interface-traps generation.

with a stress voltage less than 3.7 or 2 V, device degradation will still occur as long as maximum electric field in channel E_m remains large. An energy band diagram is more useful to explain the phenomenon, which is shown in Fig 1.15.

1.3.2 Hot Carrier Induced Device Degradation Model

Device parameters are changed during stress because of the hot-carrier induced interface traps. The parameter degradation shows up in some basic parameters including increase in threshold voltage ΔV_{th} [24], reduction in the transconductance in the linear or saturation region ΔG_m [24], and the reduction in electron mobility μ_0 [26].

An empirical model for the device degradation due to hot-carrier injection under the stress condition is presented in [24]. The device degradation (V_{th} or G_m shift) is shown as a function of stress time with the drain voltage, V_D as a parameter. The device degradation follows a power law behavior expressed as follows:

$$\Delta V_{th} \text{ (or } \Delta G_m / G_{m0}) = At^n \quad (1.13)$$

The parameter n in Eq. (1.13) is strongly dependent on the gate voltage, V_G but has insignificant dependence on the drain voltage, V_D . In the case of drain avalanche hot-carrier injection, which causes the maximum degradation, n is chosen to be 0.5-0.75 according to [24, 25]. The parameter, A is the magnitude of degradation which is strongly dependent on V_D and has also insignificant dependence on V_G and is described by

$$A \propto \exp(-\alpha/V_D) \quad (1.14)$$

This equation is valid over wide ranges of L_{eff} and t_{ox} .

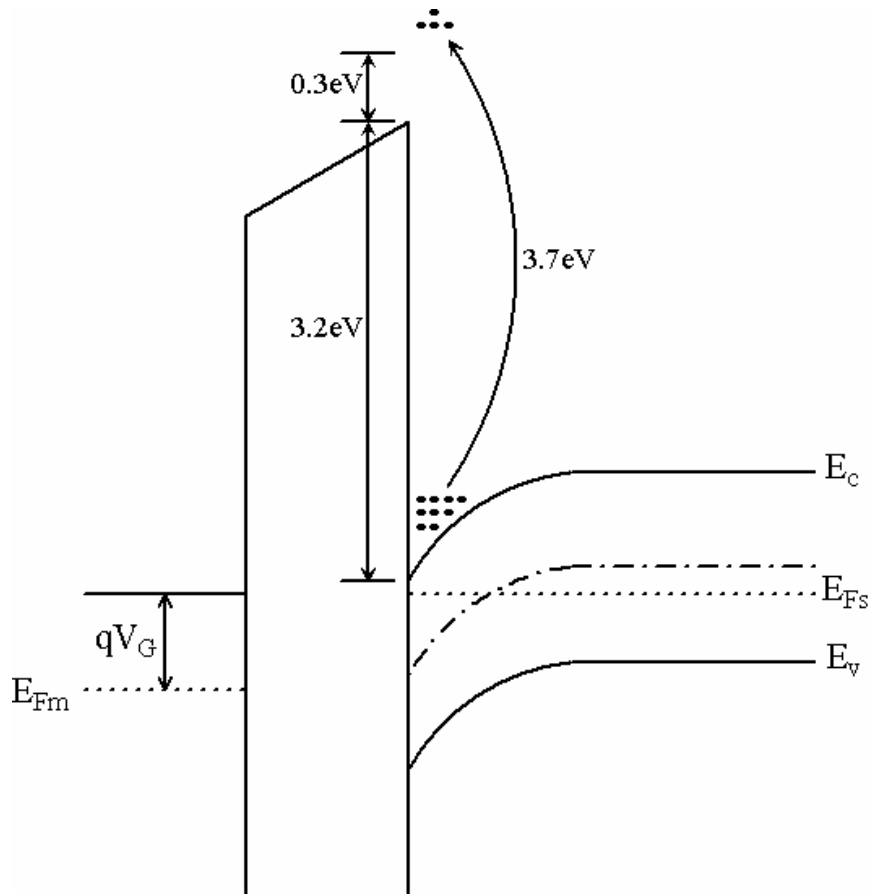


Figure 1.15: Energy band diagram of an nMOSFET under stress condition.

The mobility degradation is reported in [26, 29], which follows a saturated power-law shown in [29]. Some experimental results are shown in [26], which have been verified by the degradation of the extracted parameters of the BSIM3v3 model. The threshold voltage increases by 40% and the mobility decreases by 45% after 4 hours of stress.

1.4 Goals and Objectives

In the following chapters, simulation results on phase noise and jitter performance in VCO and PLL circuits are presented. Circuit designs of different VCO and PLL structures are described. Phase noise and jitter measurement setup and experimental results are given. Design strategies for low noise, high speed submicron CMOS PLL circuits may be developed based on the noise studies in this dissertation.

Chapter 2 discusses the VCO phase noise and jitter performance degradation considering the hot carrier effect. Degradation model and simulation results on phase noise and jitter degradation on different type of VCOs are shown. Single-ended current starved VCOs with hot carrier stress operation mode are designed and fabricated in 0.5 μm N-well CMOS process. Jitter measurement setup and experimental results on single-ended current starved VCOs before and after hot carrier stress are presented.

Chapter 3 extends the noise studies of VCO discussed in Chapter 2 to a PLL circuit. PLL phase noise and jitter prediction methods are proposed. VCO gain degradation due to hot carrier effect is studied and applied to the PLL circuit. Simulation studies of hot carrier induced degradation on PLL transient response, phase noise and jitter performance are demonstrated.

Chapter 4 investigates the PLL phase noise graphical prediction method. Two PLL circuits with different VCOs are designed and fabricated in 0.5 μm N-well CMOS process. Phase noise measurement results of open loop VCOs and PLLs are presented. The experimental results

closely match the predicted PLL phase noise curve, which verifies the graphical prediction method.

Chapter 5 proposes a 3 GHz adaptive bandwidth LC tank VCO based PLL circuit with tunable loop components and investigates its noise properties. Phase noise performance changes due to the variation of PLL loop components are studied. PLL phase noise optimization based on tunable loop components is discussed. Moreover, the impact of Q-factor for spiral inductor on PLL phase noise performance is presented.

Chapter 6 provides a summary of the work presented and scope for future work.

Appendix A presents the MOSIS level 8 model parameters for both 0.5 and 0.25 μm CMOS technology circuit simulations using SPICE.

Appendix B demonstrates the derivations of jitter and phase noise model in ring oscillators and the phase noise prediction for PLL.

Appendix C gives the list of publications.

Appendix D is the permission to use copyrighted materials.

CHAPTER 2*

PHASE NOISE AND JITTER STUDY IN CMOS VOLTAGE-CONTROLLED OSCILLATOR (VCO) CONSIDERING HOT CARRIER EFFECTS

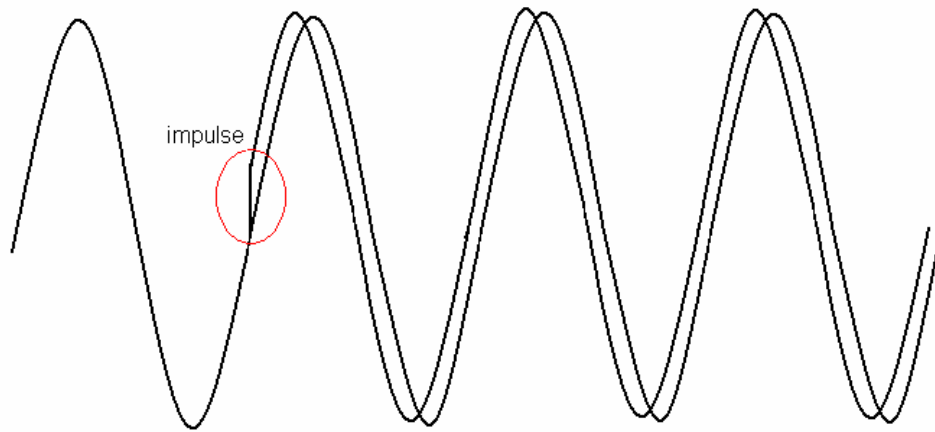
A voltage-controlled oscillator (VCO) is the essential building block in a phase-locked loop (PLL) which is used in almost every synchronous digital system. As one of the most significant parts in PLL, VCO also plays a dominant role in PLL noise issues. To study the phase noise and jitter of a PLL, understanding of the noise properties of VCO is very crucial. In this Chapter, phase noise and jitter models for VCO are presented based on the noise model of MOSFETs used in the ring oscillator. Moreover, for submicron CMOS VCO, hot-carrier effect or hot-electron induced device degradation is considered in this work to study the VCO noise degradations. Simulation results are based on the 0.5 μm CMOS model parameters listed in Appendix A. Measurement results of jitter degradation are also presented.

2.1 Phase Noise and Jitter in Ring Oscillators

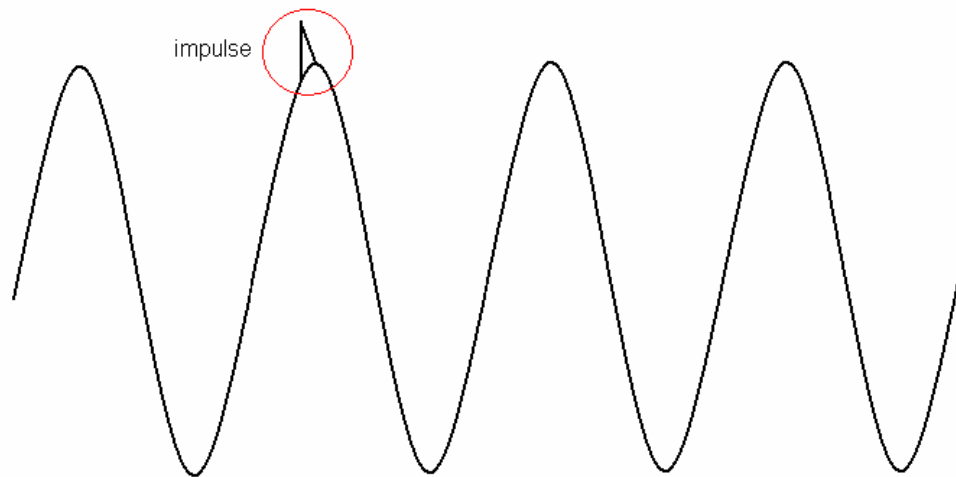
The phase noise and jitter of an oscillator are modeled by the time-variant model through an impulse response method [15, Appendix B]. In an inverter-chain type CMOS ring oscillator, the phase noise and jitter are caused by a current impulse at one of its electrical nodes. There are two extreme cases for the impulse injection. In one of the case, the current impulse is injected during a transition as shown in Fig. 2.1(a) which results in a large phase shift. In the other case, the current impulse is injected when the node is saturated either with the supply voltage or the ground as shown in Fig. 2.1(b) and the impulse will have a minimal effect on the phase shift.

* Part of this work is reported in following publications:

1. C. Zhang and A. Srivastava, "Hot carrier effects on jitter performance in CMOS voltage-controlled oscillators," *Fluctuations and Noise Letters*, Vol. 6, No. 3, pp. L329-L334, 2006.
2. C. Zhang and A. Srivastava, "Hot carrier effects on jitter and phase noise in CMOS voltage-controlled oscillators," *Proceedings of SPIE – Noise in Devices and Circuits III*, Vol. 5844, pp. 52-62, May 2005.



(a)



(b)

Figure 2.1: Effect of impulses injected during (a) transition and (b) peak.

A model has been developed for the jitter and phase noise in CMOS ring oscillator circuits assuming thermal noise as the dominant noise source [15]. For MOS transistors, assuming thermal noise is dominant, the drain current noise spectral density is given by [15]

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma\mu C_{ox} \frac{W}{L} \Delta V \quad (2.1)$$

where k is the Boltzmann constant, T is the temperature in Kelvin, μ is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are the effective channel width and length of the device, respectively, and ΔV is the gate voltage overdrive, $\Delta V = V_{gs} - V_{th}$. The coefficient γ , which characterizes the noise ratio between the saturation and linear regions, is 2/3 for long-channel devices in the saturation region and two to three times greater for short-channel devices. In this work, γ is taken to be 4/3 for all MOSFETs [15].

2.1.1 Phase Noise and Jitter Analysis for Single-Ended Ring Oscillator

Figure 2.2 shows the circuit diagram of a single-ended CMOS ring oscillator where both NMOS and PMOS transistors have the same channel length. The maximum phase shift and the resulting maximum noise result when input and output nodes of an inverter in the ring oscillator are at $V_{DD} / 2$. The maximum noise resulting from NMOS and PMOS transistors is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma\mu_{eff} C_{ox} \frac{W_{eff}}{L} \Delta V \quad (2.2)$$

where

$$W_{eff} = W_n + W_p \quad (2.3)$$

$$\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p} \quad (2.4)$$

and

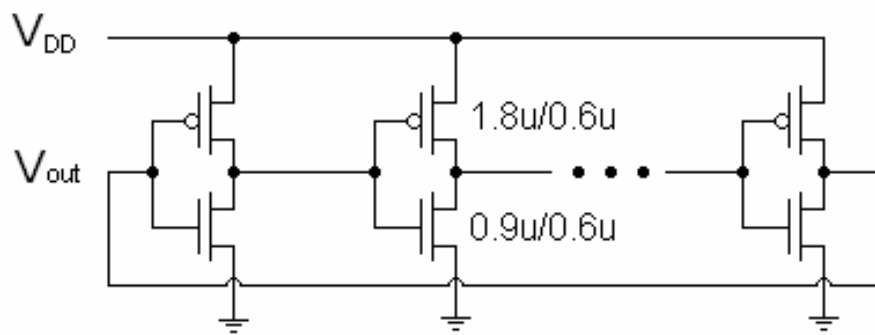


Figure 2.2: Circuit diagram of a single-ended ring oscillator.

$$\Delta V = V_{DD} / 2 - V_{th} \quad (2.5)$$

In an N-stage single-ended ring oscillator, the total power dissipation is approximately given by

$$P = 2\eta N V_{DD} q_{\max} f_0 \quad (2.6)$$

where q_{\max} is the maximum total charge stored on each node of the ring oscillator, η is a proportionality constant which is used to describe the relationship between the normalized stage delay and the maximum slope of the normalized waveform. Assuming $\mu_n W_n = \mu_p W_p$ to make the waveforms symmetric, the frequency of oscillation can be approximated by

$$f_0 = \frac{1}{\eta N (t_r + t_f)} \approx \frac{\mu_{\text{eff}} W_{\text{eff}} C_{OX} \Delta V^2}{8\eta N L q_{\max}} \quad (2.7)$$

where t_r and t_f are the rise and fall time, respectively, associated with the maximum slope during a transition.

The phase noise and jitter in a single-ended ring oscillator shown in Fig. 2.2 are given by [15]

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}} \cdot \frac{f_o^2}{\Delta f^2} \quad (2.8)$$

$$\sigma_{\Delta T} = \kappa \sqrt{\Delta T} \quad (2.9)$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \quad (2.10)$$

where $L\{\Delta f\}$ describes the phase noise and $\sigma_{\Delta T}$ represents the RMS jitter, P is the total power dissipation of the oscillator, f_0 is the oscillation frequency, η is the proportionality constant relating the rise time and the stage delay of the oscillator which can be taken as 0.75 [15]. In Eq.(2.9), κ is the jitter proportionality constant. V_{char} in Eqs. (2.8) and (2.10) is the characteristic voltage of the device, defined as $V_{char} = \Delta V / \gamma$. As shown in Fig. 2.1 (a), the

maximum phase shift occurs when the current is injected during the transition. Therefore, the gate overdrive voltage, $\Delta V = V_{DD}/2 - V_{th}$ is a reasonable choice for the worst case noise analysis.

2.1.2 Phase Noise and Jitter Analysis for Differential Ring Oscillator

Similarly, the phase noise and jitter analysis of a differential ring oscillator is also carried out. Figure 2.3 shows the circuit diagram of a differential CMOS ring oscillator. The total power dissipation is given by

$$P = NI_{tail}V_{DD} \quad (2.11)$$

where I_{tail} is the tail bias current of the differential pair. The frequency of oscillation can be approximated by

$$f_0 = \frac{1}{2Nt_D} \approx \frac{1}{2\eta Nt_r} \approx \frac{I_{tail}}{2\eta Nq_{max}} \quad (2.12)$$

where t_D is the delay of each stage. The total current noise on each node is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kTI_{tail} \left(\frac{1}{V_{char}} + \frac{1}{R_L I_{tail}} \right) \quad (2.13)$$

where R_L is the effective load resistance, and can be approximated by

$$R_L = \frac{1}{\mu_p C_{OX} \frac{W_p}{L_p} (|V_{gs}| - |V_{thp}|)} \quad (2.14)$$

and $V_{char} = \Delta V / \gamma$. The expressions for the phase noise and the proportionality constant in Eq.

(2.9) of jitter for an N-stage differential CMOS ring oscillator are given by

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right) \cdot \frac{f_o^2}{\Delta f^2} \quad (2.15)$$

and

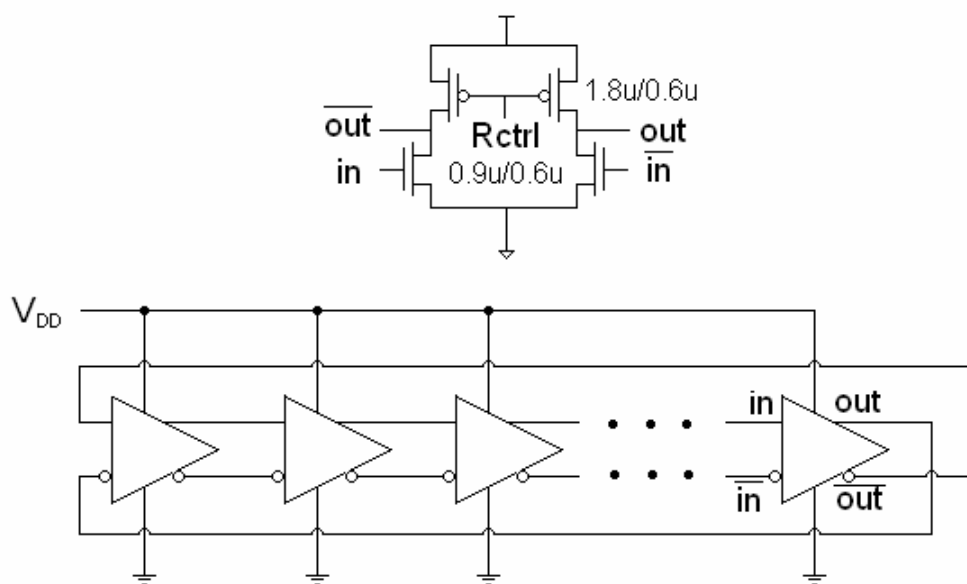


Figure 2.3: Circuit diagram of a differential ring oscillator.

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right)} \quad (2.16)$$

where $V_{char} = \Delta V / \gamma$, and $\Delta V = (V_{DD} / 2) - V_{th}$ gives the maximum phase shift as discussed for the single-ended ring oscillator circuit. In comparison to the single-ended ring oscillator, the differential ring oscillator shows a phase noise dependency on the number of stages, N.

2.2 Hot Carrier Induced Degradation on Jitter and Phase Noise in VCO

Some work related to hot-carrier studies in VCO have been reported in [29, 30]. In this work, the effect of hot carrier stress on CMOS voltage-controlled oscillators (VCOs) is investigated. A model of the threshold voltage degradation in MOSFETs due to hot carrier stress has been used to model jitter and phase noise in voltage-controlled oscillators. The relationship between the stress time which induces the hot carrier effects and the degradation of the VCO performance is presented. The VCO performance degradation takes into consideration decrease in operation frequency, increase in jitter and phase noise and decrease in tuning range. The VCO circuits have been designed in 0.5 μm n-well CMOS technology for operation at 3 V.

2.2.1 Modified VCO Phase Noise and Jitter Model after Stress

The jitter and phase noise change due to V_{th} shift since V_{char} depends on V_{th} through the following equations: $V_{char} = \Delta V / \gamma$ and $\Delta V = (V_{DD} / 2) - V_{th}$. The modified expression for V_{char} after hot carrier stress is given by

$$V_{char} = \frac{(V_{DD} / 2) - V_{th} - \Delta V_{th}}{\gamma} \quad (2.20)$$

The modified expressions of phase noise and the jitter proportionality constant in single-ended and differential ring oscillators are given as follows:

For a single-ended ring oscillator

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{\gamma \cdot V_{DD}}{V_{DD}/2 - V_{th} - \Delta V_{th}} \cdot \frac{f_o^2}{\Delta f^2} \quad (2.21)$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{\gamma \cdot V_{DD}}{V_{DD}/2 - V_{th} - \Delta V_{th}}} \quad (2.22)$$

and for a differential ring oscillator

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{\gamma \cdot V_{DD}}{V_{DD}/2 - V_{th} - \Delta V_{th}} + \frac{V_{DD}}{R_L I_{tail}} \right) \cdot \frac{f_o^2}{\Delta f^2} \quad (2.23)$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{\gamma \cdot V_{DD}}{V_{DD}/2 - V_{th} - \Delta V_{th}} + \frac{V_{DD}}{R_L I_{tail}} \right)} \quad (2.24)$$

where ΔV_{th} is a function of the stress time, t . Since the VCO designs are based on the ring oscillator design, the phase noise and jitter in a VCO circuit are also dependent on stress conditions for hot carrier effects. Moreover, hot carrier stress also affects the oscillation frequency which shows a decreasing trend. Consequently, the device degradation also results in decrease of the VCO tuning range.

2.2.2 Simulation Results

Three different types of oscillator circuits, a single-ended ring oscillator, a differential VCO and a current-starved VCO, have been designed as shown in Figs. 2.2, 2.3 and 2.4, respectively. With different number of stages for each type of VCO, the relationship between the performance of VCO and the number of stages, N are studied.

The device degradation including decrease in oscillation frequency, decrease in VCO tuning range, increase in jitter and phase noise has been simulated in SPICE using level 8 CMOS parameters [Appendix A]. While the degradation in phase noise performance is modeled using Eqs. (2.21) and (2.23). Due to the limitation on the hot carrier stress simulation, the SPICE simulation is realized by adjusting the model parameter of threshold voltage according to the hot

carrier degradation model described in the previous section. The threshold voltage may increase by 120 mV after four hours stress [29].

Figures 2.5 - 2.7 show the simulation results of the hot carrier induced degradations in different aspects. Figures 2.5 (a) and (b) show the variation of oscillation frequency and tuning range change with the control voltage due to hot carrier effects for the current-starved VCO and the differential VCO, respectively. For the current-starved VCO, the oscillation frequency decreases by more than 80 MHz in 2.2 V - 3 V range of control voltage. The tuning range decreases from 72 MHz-287 MHz to 65.4 MHz-201 MHz which is nearly 37%. In differential VCO, maximum reduction in oscillation frequency is observed at 0.5 V control voltage and is ~ 100 MHz. The tuning range decreases from 32 MHz-983 MHz to 26 MHz to 698 MHz, which is about 30%.

Figures 2.6 (a) and (b) show the variation of phase noise as a function of stress time with different central frequency for the single-ended current-starved VCO and the differential VCO at 1 MHz offset frequency, respectively. The corresponding variations of phase noise power spectrum density due to the hot carrier stress are shown in Figs. 2.7 (a) and (b), respectively.

SPICE simulation show that due to the hot carrier effect, for the single-ended ring oscillator, the phase noise changes from -104 dBc to -105 dBc at 1 MHz frequency offset with a power dissipation of 0.37 mW. For the current-starved VCO, the phase noise changes from -109 dBc to -107 dBc at 1 MHz offset from the center frequency, 200 MHz; for the double-ended differential VCO, the tuning range changes from 32 MHz - 983 MHz to 26 MHz - 698 MHz, and phase noise changes from -86 dBc to -87 dBc at 1 MHz offset from the center frequency, 700 MHz. The results show that the hot carrier induced degradation on phase noise of ring oscillator is not significant. That's because the oscillation frequency also degrades after hot carrier stress, but the oscillation frequency is fixed during the phase noise comparison.

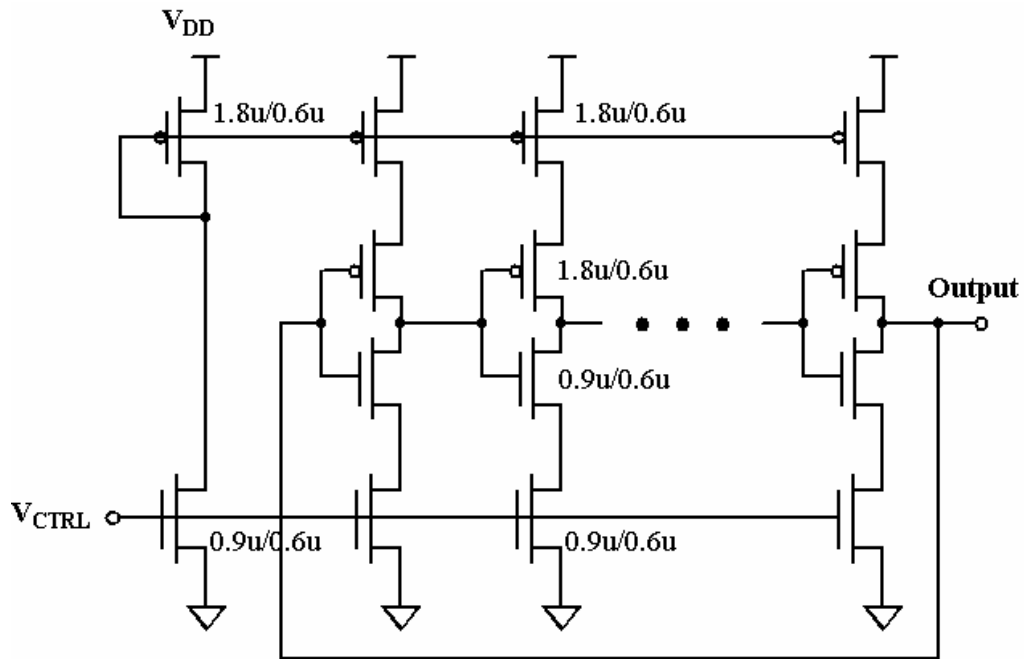
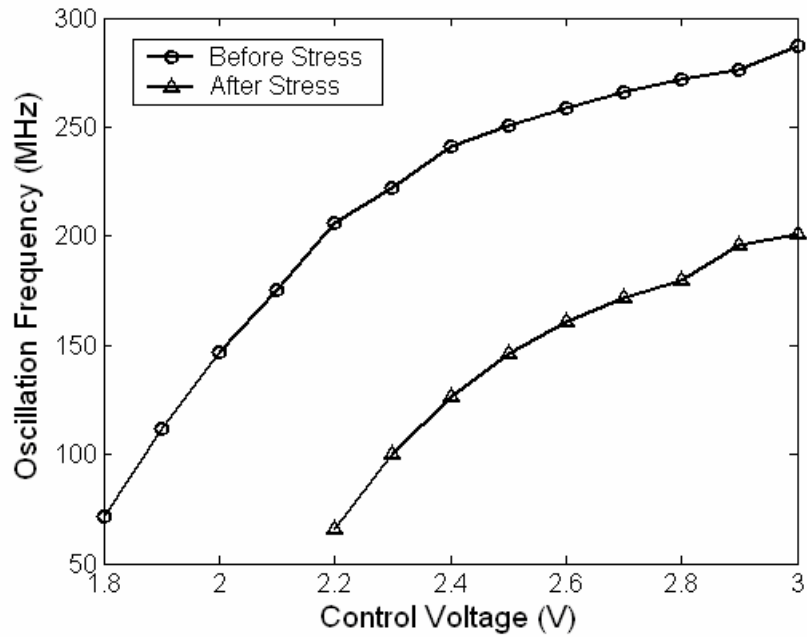
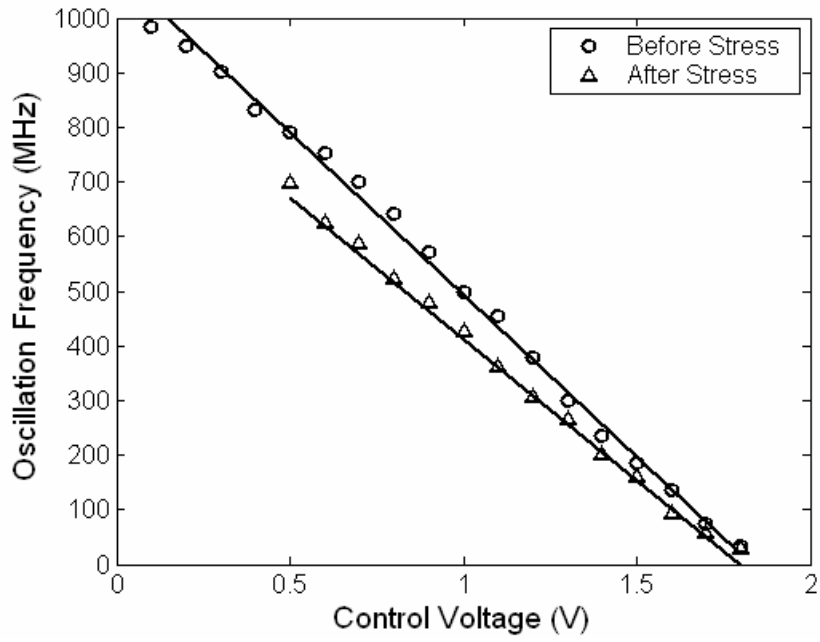


Figure 2.4: Circuit diagram of a current starved VCO.

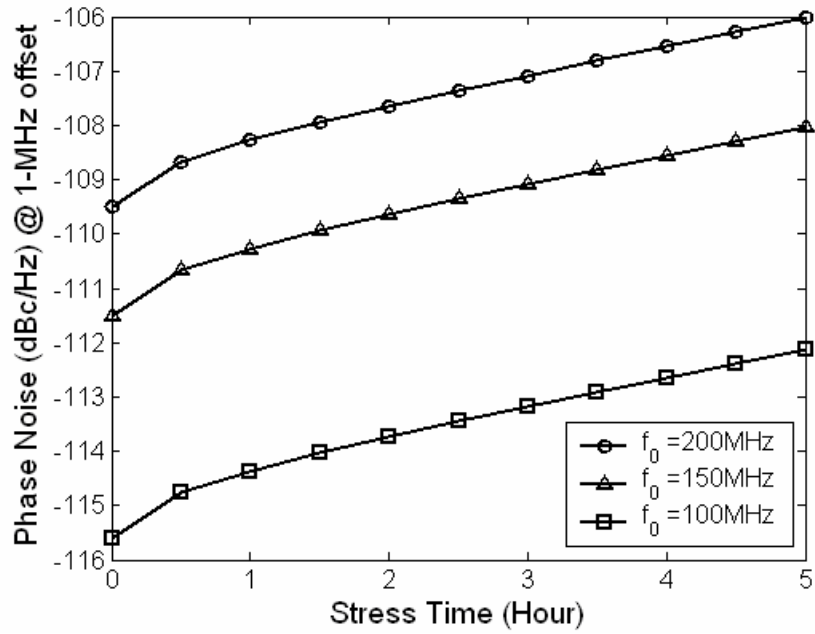


(a)

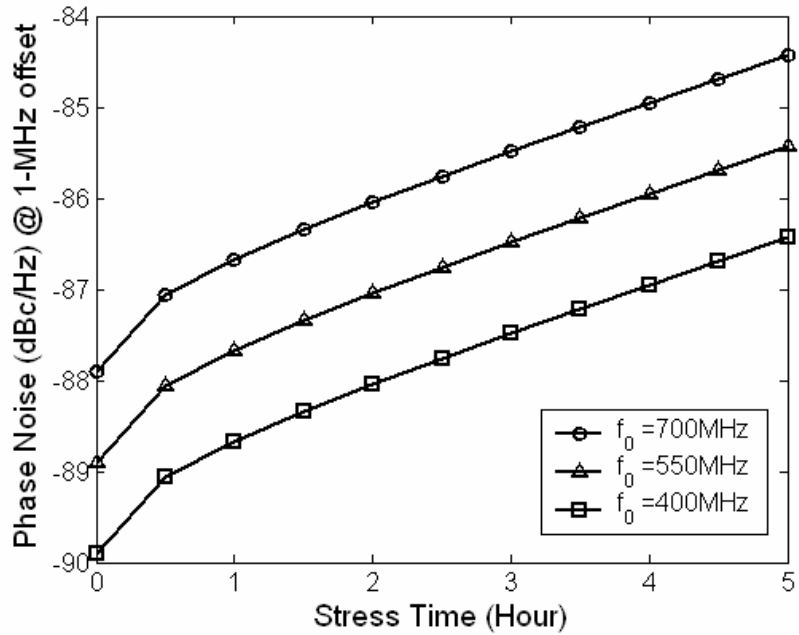


(b)

Figure 2.5: Hot carrier induced degradation on tuning characteristic of (a) the single-ended current starved VCO and (b) the differential VCO.

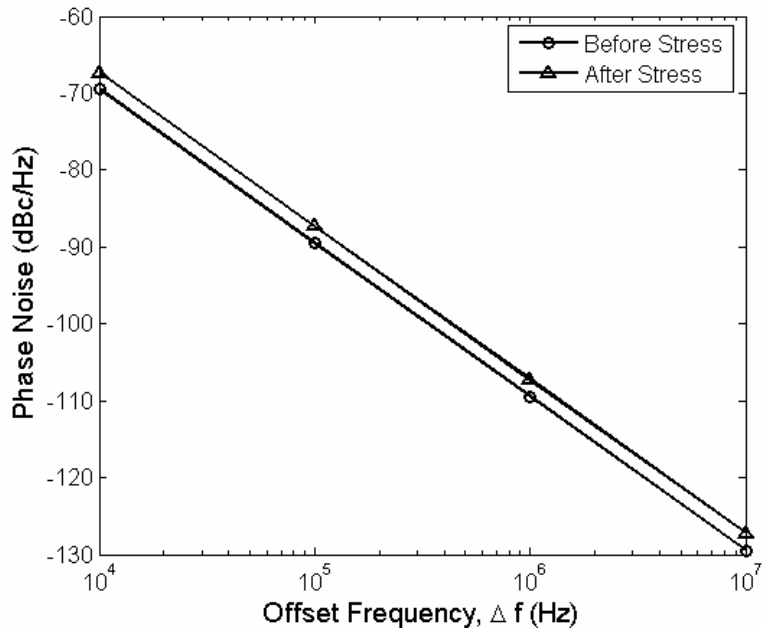


(a)

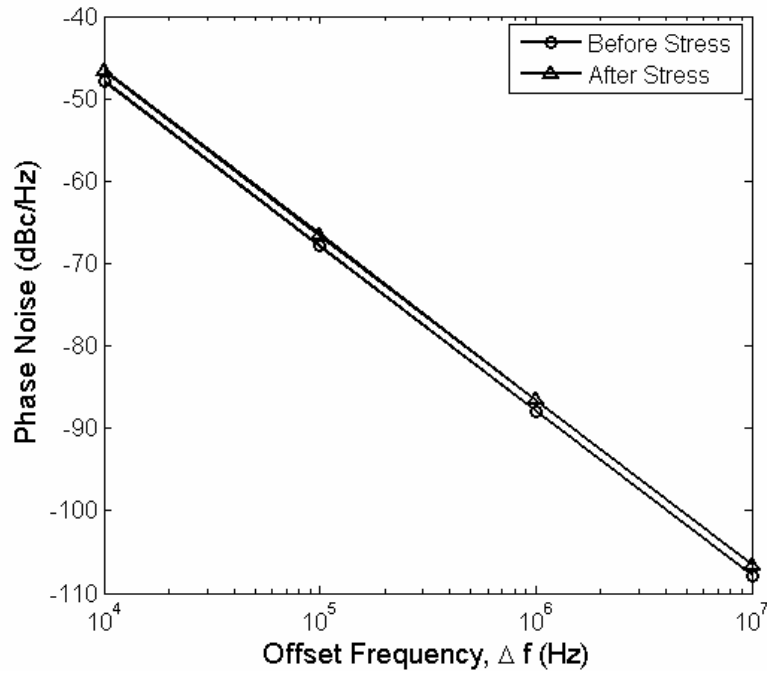


(b)

Figure 2.6: Hot carrier induced degradation on phase noise at 1 MHz offset frequency at different center frequency for (a) the single ended-current starved VCO and (b) the differential VCO.



(a)



(b)

Figure 2.7: The variation of phase noise power spectrum density due to the hot carrier stress for (a) the single-ended current starved VCO and (b) the differential VCO.

2.3 Jitter Measurement and Discussion

In the above section, only the simulation results of phase noise in different VCOs are presented which is not sufficient to verify the hot electron induced noise degradation. Simulation and measurement results of jitter performance before and after hot carrier stress is presented in this section. Figure 2.8 shows the circuit diagram of a single-ended current starved VCO with two modes of operations for hot carrier stress study. The two operation modes are the stress mode and the oscillation mode. Switching between these two modes is realized by a mode control signal, V_{mode} . In the operation mode, both V_{stress} and V_{mode} are connected to ground. The switching n-MOSFETs, which connect V_{stress} to each oscillating node, are in cutoff. Thus, transistors in the oscillator are not stressed. In the stress mode, V_{mode} is connected to V_{DD} , which turns-on the switching n-MOSFETs. V_{stress} is set to a voltage higher than the expected voltage to be stressed on the gate and drain of each n-MOSFET in the oscillator. By adjusting V_{stress} and measuring V_{out} of the VCO, the different stress voltages can be set. The VCO does not oscillate during the stress time but hot carriers are induced in this period.

The maximum lateral channel electric field E_m can be approximately calculated using equation [25]:

$$E_m = \frac{V_D - V_{D.sat}}{l} \quad (2.25)$$

where $V_{D.sat}$ is the potential at the pinch off, V_D is the drain stress voltage and l is the length of pinch off region which is approximately given by $l = \sqrt{3t_{ox}x_j}$ [25]. t_{ox} is the oxide thickness which is 14.2 nm, and x_j is the junction depth which is 150 nm for 0.5 μm CMOS process. Therefore, l is approximated as 80 nm. One simple model for $V_{D.sat}$ is shown below [25]:

$$V_{D,sat} = \frac{(V_G - V_{th})LE_{sat}}{V_G - V_{th} + LE_{sat}} \quad (2.26)$$

where E_{sat} is the critical field for velocity saturation, about $5 \times 10^4 V/cm$. In this work, channel length is $0.5 \mu m$, threshold voltage is $0.6 V$, gate stress voltage is $3 V$ which result in $V_{D,sat} = 1.2 V$. For $3 V$ drain stress voltage, the maximum lateral channel electric field E_m is approximately $2.3 \times 10^5 V/cm$. Note that E_m cannot be determined accurately by experiments, or even simulations [25], however, the E_m estimation in this work provide a clear relationship between gate, drain stress voltage and the channel electric field. For a given E_m for hot electron generation, the stress voltage on gate and drain can be easily calculated.

Different CMOS VCOs with stress mode of operation are fabricated in $0.5 \mu m$ n-well CMOS process. A 5 stage and 15 stage VCOs are the most fully functional circuit blocks in the chip. These two VCOs are selected for the jitter measurements to investigate the jitter degradation due to hot carrier effect. Hot carrier stress was applied during the stress mode of operation. The layout and die photograph of the chip and the 15 stage single-ended current starved VCO are shown in Figs. 2.9 and 2.10, respectively. Jitter measurements are performed by using a digital sampling oscilloscope with the histogram mode and color grading mode. A delay unit in front of the sampling head is needed for the minimum delay requirement for trigger transition and the first acquired sample [15].

In this work, two SMA cables with different length are used for SD-24 sampling head and the trigger which satisfy the minimum delay requirement [42]. Figure 2.11 shows the jitter measurement setup. Figure 2.12 shows the digital sampling oscilloscope Tek11801A jitter measurement display. The jitter is measured for the second rising edge which gives a measurement interval of one clock period.

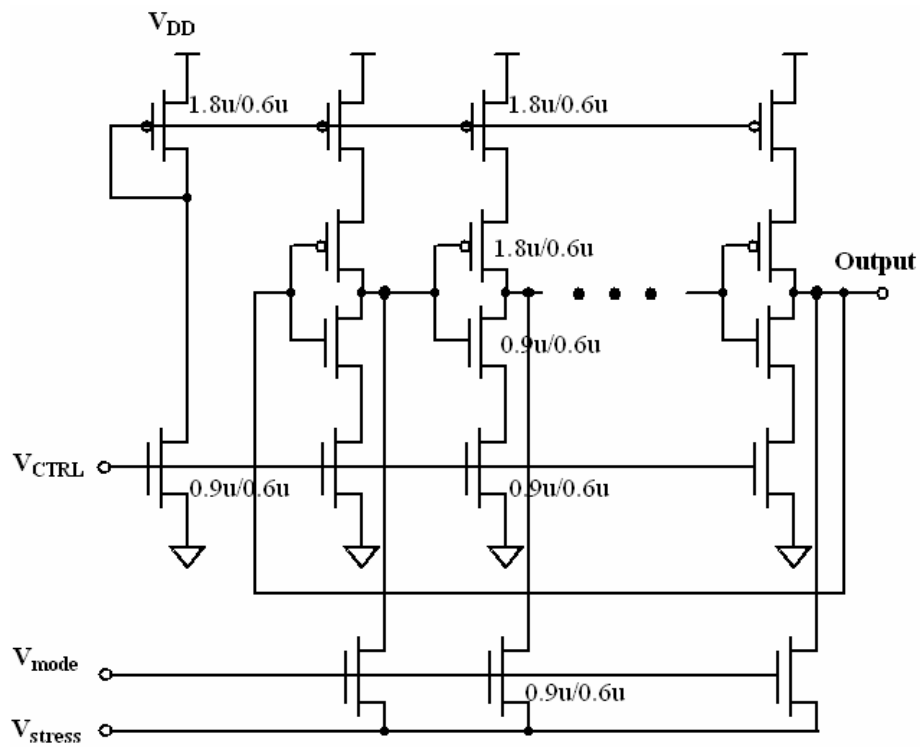
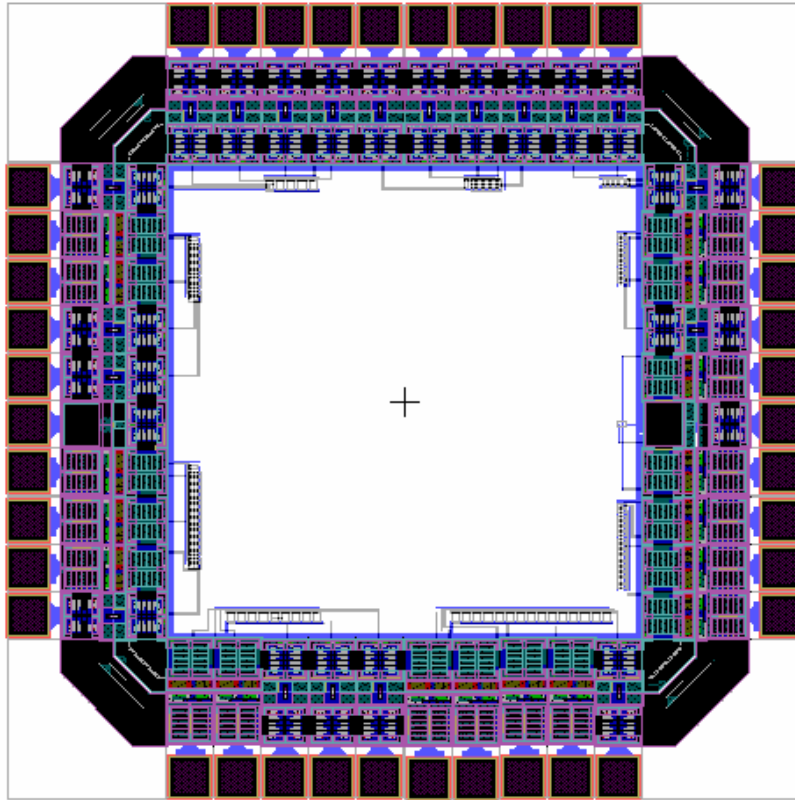
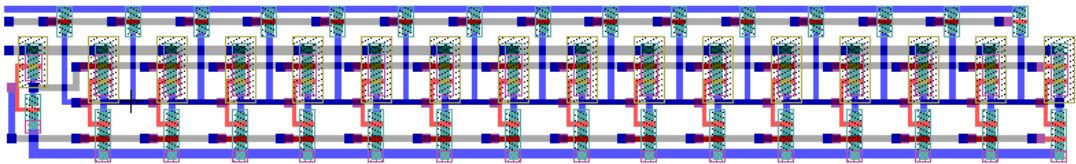


Figure 2.8: The circuit diagram of a single-ended current starved VCO with operation mode and hot carrier stress mode.



(a)



(b)

Figure 2.9: The layout of (a) whole chip, (b) a 15 stage current starved VCO.

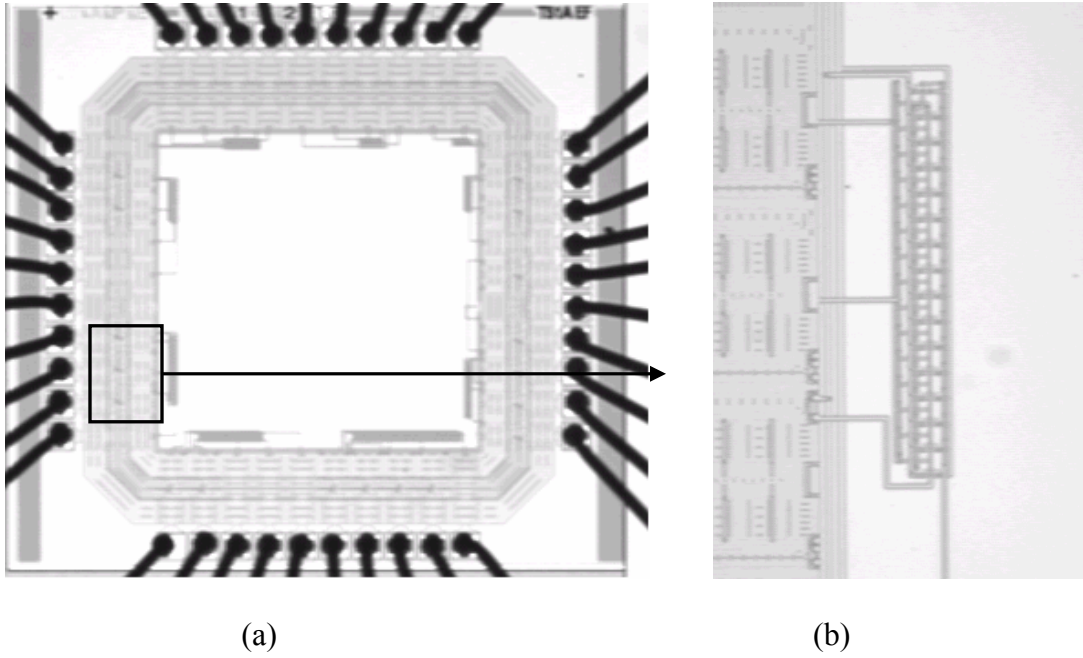


Figure 2.10: The die photograph of (a) whole chip, (b) a 15 stage current starved VCO.

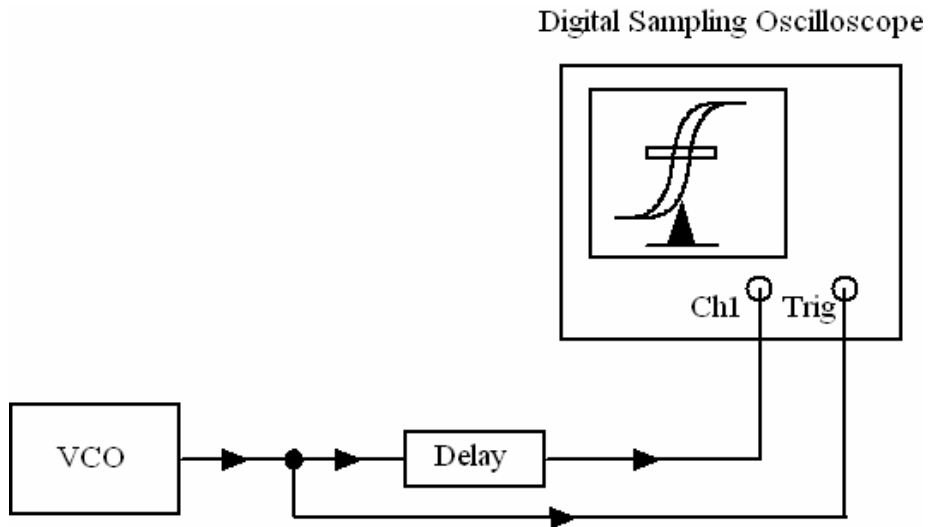
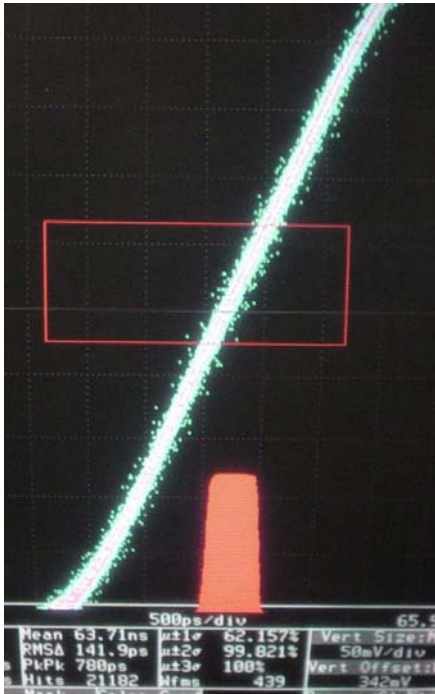
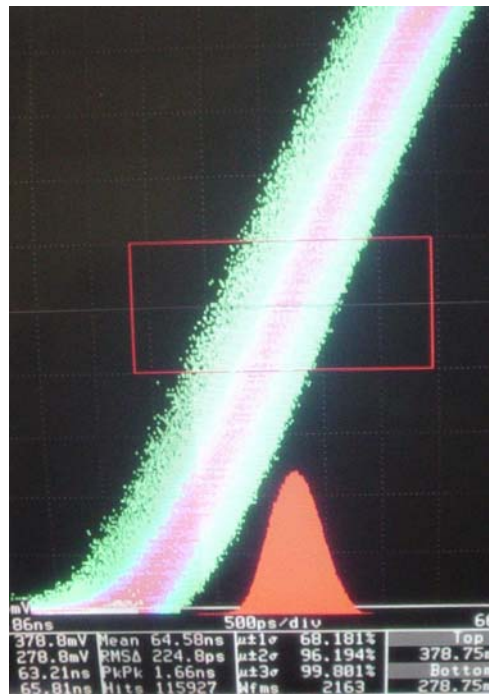


Figure 2.11 The setup for VCO jitter measurement using the digital sampling oscilloscope Tek 11801A with 6.9 ns delay calculated [42] between trigger and signal.



(a)



(b)

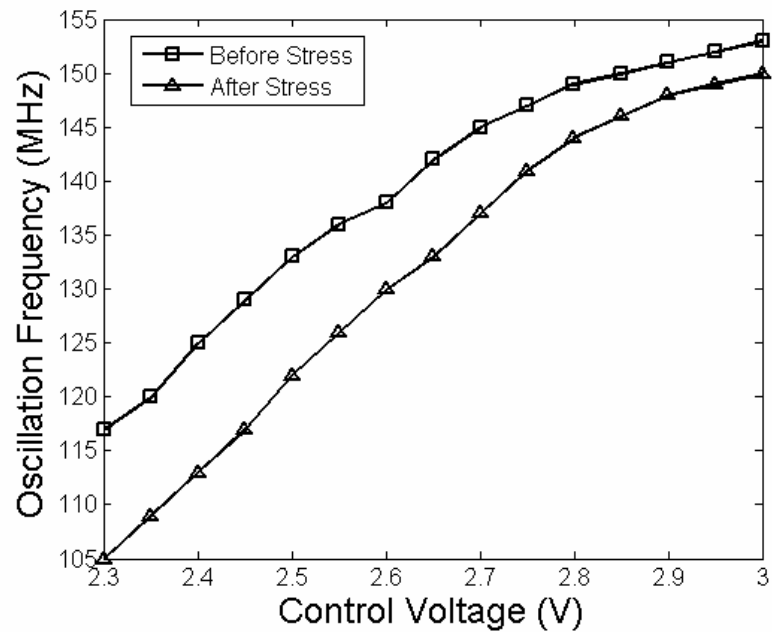
Figure 2.12: The histogram of jitter measurement (a) for a 15 stage single-ended oscillator, (b) for a 15 stage current starved VCO.

Measurement results on these two current starved VCOs show that the oscillation frequency decreased by around 5 MHz. And a 40 ps increase in RMS jitter was observed after four hours hot carrier stress for both VCOs. The degradation on oscillation frequency and jitter performance due to hot carrier stress are shown in Figs. 2.13 (5 stage VCO) and 2.14 (15 stage VCO), respectively.

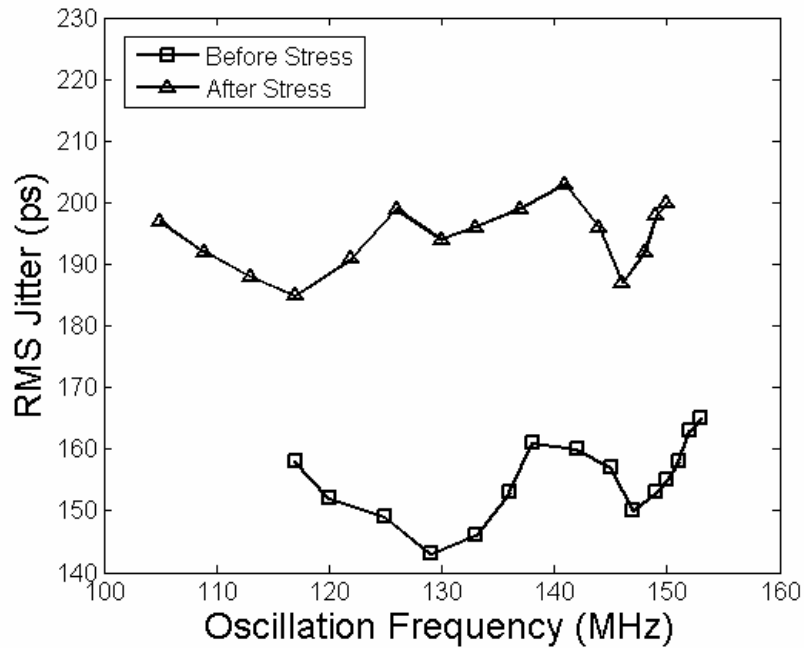
The experiment results of the degradation in jitter with stress time as a parameter is shown in Fig. 2.15 by taking the average RMS jitter measured under different stress times. The normalized simulation results are also shown in this figure. Although difference between the absolute value of measured jitter and the simulated jitter can be observed through the experiment, the increasing trend in jitter can be definitely proved by matching with normalized simulation results. The jitter data difference may be caused by the capacitance of the bonding pads and the interconnections. Moreover, the underestimation on the measurement interval may be another factor causing the difference.

2.4 Summary

The jitter and phase noise in CMOS voltage-controlled oscillators (VCOs) are modeled after the hot carrier stress. The VCO performance degradation including decrease in the operation frequency, decrease in the tuning range and increase in jitter and phase noise is simulated in SPICE using the device degradation model due to hot carrier stress. The comparison of phase noise before and after the hot carrier stress was performed by fixing the oscillation frequency. The phase noise models developed in the present work can be very useful in phase noise analysis for CMOS based OFDM systems based on hot carrier effects as reported in recent publications [34-38]. Furthermore, different CMOS VCOs with the oscillation mode and hot carrier stress mode are designed in 0.5 μm n-well CMOS process. The comparison of tuning characteristic and jitter performance before and after the hot carrier stress was performed.

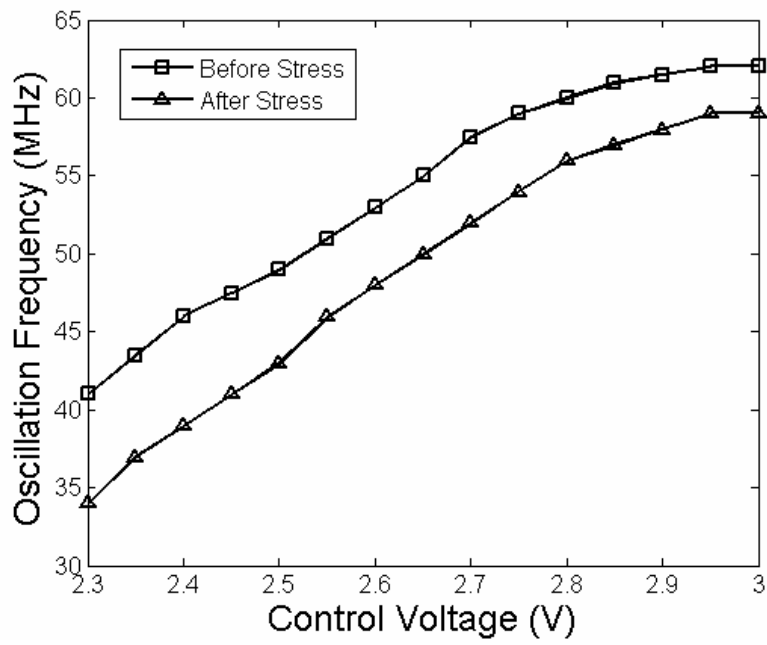


(a)

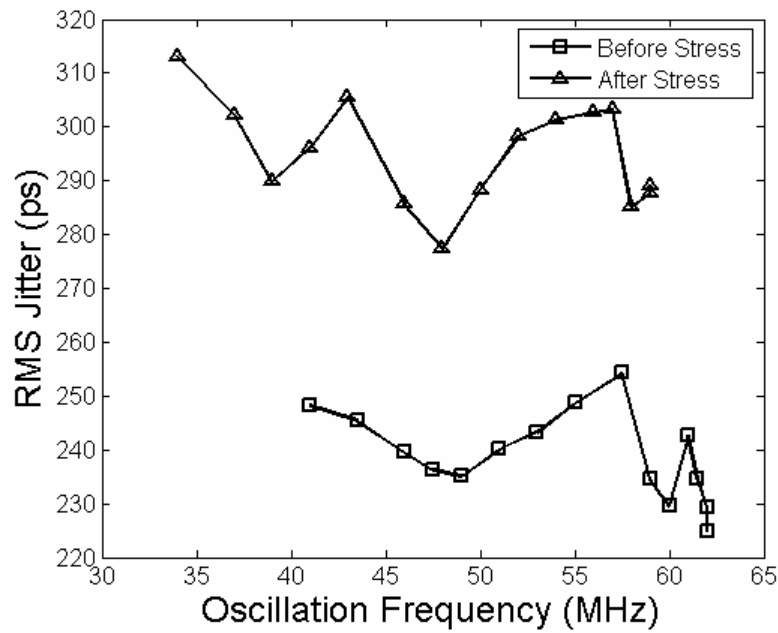


(b)

Figure 2.13: The degradation on (a) oscillation frequency, (b) jitter performance under different oscillation frequency for a 5 stage current-starved VCO due to hot carrier effects.



(a)



(b)

Figure 2.14: The degradation on (a) oscillation frequency and (b) jitter performance under different oscillation frequency for a 15 stage current-starved VCO due to hot carrier effects.

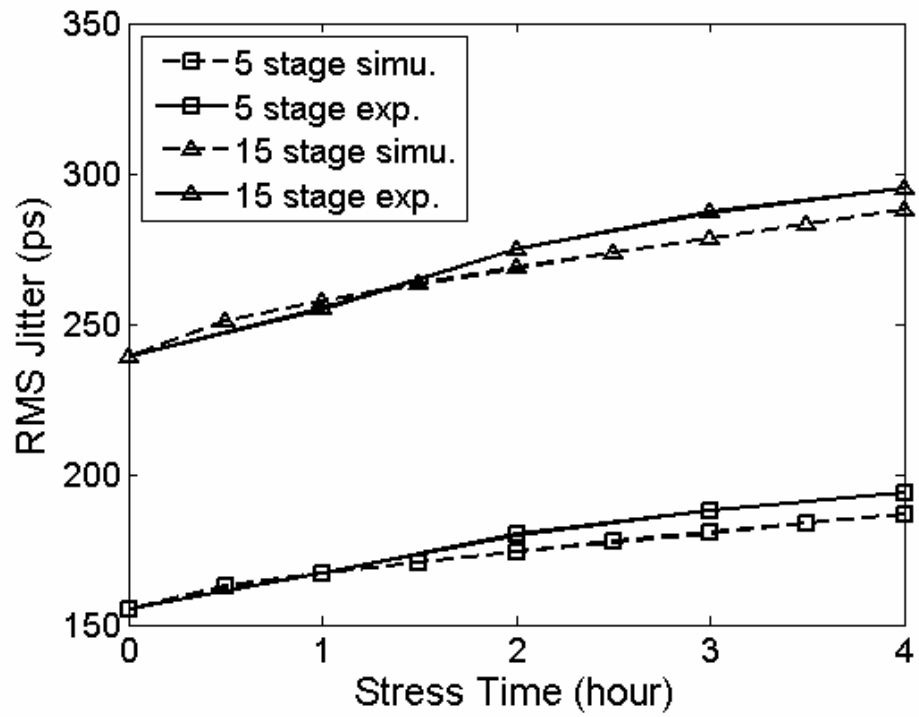


Figure 2.15: The normalized simulation results and experiment results for jitter degradation versus the hot carrier stress time for a 5 and 15 stage current-starved VCOs.

The experimental results verify the degradation in oscillation frequency and jitter performance of VCO. After four hours hot carrier stress, the oscillation frequency decreased by about 5 MHz and the RMS jitter increased by about 40 ps. Closely matching between the normalized simulation results and the experimental results verifies the jitter degradation model for single-ended current starved VCO. The results of the work would be very useful in design of robust CMOS VCO and Phase-Locked Loop circuits.

CHAPTER 3[†]

PHASE NOISE AND JITTER STUDY IN CMOS PHASE-LOCKED LOOP (PLL) CONSIDERING HOT CARRIER EFFECTS

Hot carrier induced device degradation on phase noise and jitter performance of voltage-controlled oscillators (VCOs) have been studied and presented in Chapter 2. Since VCO is one of the dominant noise sources in a PLL, the degradation on VCO affects the PLL performance including the tracking performance, and the phase noise and jitter at the output. In this chapter, the hot carrier induced degradation in VCO gain is investigated. The VCO under discussion is a single-ended current starved VCO which is designed in 0.25 μm CMOS process. The phase noise and jitter graphical treatment method is introduced. The loop dynamics, phase noise and output clock jitter of a second order PLL based on this type of VCO are studied. The loop parameters, i.e., damping factor and loop bandwidth, phase noise and jitter degradations due to VCO degradation are analyzed, considering hot-carrier effects.

3.1 Noise Properties of PLL Building Blocks

To investigate the noise properties of the PLL, it is necessary to begin with the noise properties of PLL building blocks [18]. Because the VCO and the frequency divider are the building blocks dealing with the high frequency oscillation, they are more subject to any fluctuations, such as thermal noise. These two parts have the most significant contribution to the noise of the whole PLL. The phase frequency detector, charge pump and loop filter can be designed in such a way to contribute negligible amount of noise to the PLL, thus they are not major sources of noise in a PLL. In this dissertation, only the noise properties of VCO and clock frequency divider are considered. The phase noise due to input reference noise is also studied.

[†] Part of this work is reported in following publication:

C. Zhang, A. Srivastava and H. -C. Wu, "Hot-electron induced effects on noise and jitter in submicron CMOS phase-locked loop circuits," *Proc. of IEEE 48th International Midwest Symposium on Circuits and Systems (MWSCAS05)*, pp. 507-510, 2005.

The noise properties of a VCO are modeled using a noiseless VCO with an additive noise source at its input and output. The output power spectrum can be given by [18]

$$S_{\Phi_{out}}(\omega) = \frac{2\pi^2 K_V^2 N_0}{\omega^2} \left(1 + \frac{\omega_{1/f^3}}{\omega}\right) + \frac{N_1}{2} \quad (3.1)$$

where K_V is the gain of VCO in Hz/V. ω is the offset frequency from the center frequency in rad/s. $N_0/2$ and $N_1/2$ are the double-sideband power spectral densities of the input and output white noise. And ω_{1/f^3} is the $1/f$ noise corner of the input behavioral noise source, which is equal to the $1/f^3$ noise corner of the VCO. Note that $1/f$ noise can be ignored at higher offset frequencies, thus only the phase noise in the $1/f^2$ region of VCO is considered in this work.

The frequency divider phase noise may also have a significant contribution to the phase noise of PLL. Ideally, a frequency divider reduces the inherent phase noise of the input signal by $20\log(N)$ dB due to its division feature. In a PLL, the input of the frequency divider is taken from the VCO output, and the output goes to the phase detector input. Thus, the input phase variations are multiplied by N at the output of the VCO, which is the output of the PLL. The phase noise power spectrum of the output will be N^2 times the input phase fluctuations. Therefore, the effect of an ideal frequency divider is to increase the phase noise of the input by $20\log(N)$ dB. Moreover, practical digital dividers usually have a large white noise floor at their output, which adds to the input of the phase detector. This noise floor can also add to the output phase noise of a PLL.

3.2 Phase Noise Graphical Treatment Prediction of PLL

Now consider the two dominant sources of the noise which affect the phase noise of the output, VCO phase noise and the input phase noise. Assuming that the VCO phase noise is not correlated with the phase noise of the input, the phase noise power spectrum at the output can be

calculated using superposition. The output phase noise due to each source can be evaluated independently and the total phase noise is the sum of them. This method of PLL phase noise prediction is also called the graphical treatment. More detailed derivation is presented in Appendix B.

Assuming a noiseless input and a noisy VCO dominated by its $1/f^2$ noise, the equivalent phase domain model of PLL is shown in Fig. 3.1. $n_0(s)$ is the input noise source in the equivalent noise model of a VCO. The effect of VCO phase noise can be calculated using the transfer function from $n_0(s)$ to $\Phi_{out}(s)$, which is given by

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{2\pi C_1 N}{I_{CH}} \cdot \frac{s}{s^2 / \left(\frac{K_V I_{CH}}{C_1 N} \right) + \tau s + 1} \quad (3.2)$$

Therefore, the power spectrum density of the output phase can be given by

$$S_{\Phi_{out}}(\omega) = \frac{N_0}{2} \cdot \frac{4\pi^2 C_1^2 N^2}{I_{CH}^2} \cdot \frac{\omega^2}{\left[1 - \omega^2 \cdot \left(\frac{C_1 N}{K_V I_{CH}} \right) \right]^2 + \omega^2 \tau^2} \quad (3.3)$$

or if the loop bandwidth, ω_n is applied,

$$S_{\Phi_{out}}(\omega) = \frac{N_0}{2} \cdot \frac{4\pi^2 C_1^2 N^2}{I_{CH}^2} \cdot \frac{\omega^2}{\left[1 - \left(\frac{\omega}{\omega_n} \right)^2 \right]^2 + \omega^2 \tau^2} \quad (3.4)$$

where $\omega_n = \sqrt{(K_V I_{CH}) / (N C_1)}$ is defined as the loop bandwidth of the PLL.

Assuming a noiseless VCO, the response of the loop to the phase variations in the input is evaluated. The input is usually generated by another oscillator, which will have its own phase noise characteristics. Considering the phase noise of $1/f^2$ region only, the input phase noise power spectrum can be given as $S_{\Phi_{in}}(\omega) = \alpha / \omega^2$, where α is a constant characterizing the

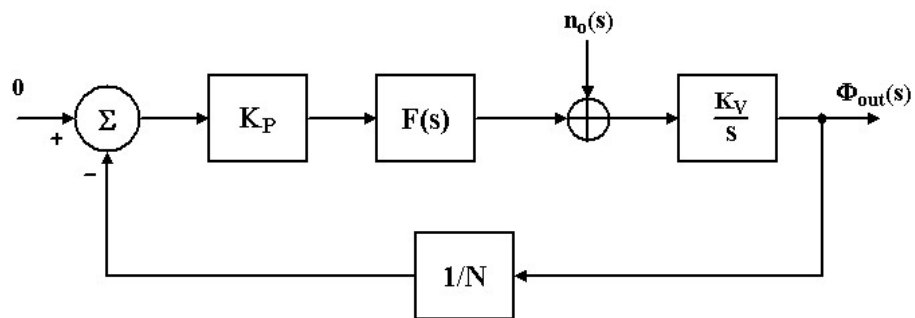


Figure 3.1: Equivalent phase domain model of PLL with VCO noise source.

phase noise of the input. For the second order PLL under consideration, the output phase noise power spectrum can be given by

$$S_{\Phi_{out}}(\omega) = \frac{\alpha}{\omega^2} \cdot \frac{\omega^2 \tau^2 + 1}{\left[1 - \omega^2 \cdot \left(\frac{C_1 N}{K_V I_{CH}} \right) \right]^2 + \omega^2 \tau^2} \quad (3.5)$$

or

$$S_{\Phi_{out}}(\omega) = \frac{\alpha}{\omega^2} \cdot \frac{\omega^2 \tau^2 + 1}{\left[1 - \left(\frac{\omega}{\omega_n} \right)^2 \right]^2 + \omega^2 \tau^2} \quad (3.6)$$

The PLL phase noise power spectrum density for a noisy VCO and ideal input reference is shown in Fig. 3.2. The PLL phase noise power spectrum density for a noiseless VCO and noisy input reference is shown in Fig 3.3. The total phase noise power spectrum of the PLL output is the sum of the phase noise evaluated by a noisy VCO and a noisy input reference independently.

Moreover, considering the noise floor introduced by the frequency divider, the total phase noise power spectrum of the PLL is shown in Fig. 3.4. As shown in this figure, input reference noise is more dominant at small offset frequency while VCO noise is more dominant at moderate offset frequency around loop bandwidth due to the peak induced by the VCO noise. At large offset frequency, the frequency divider is dominant because of its flat feature. As a result, at small offset frequency, the PLL phase noise is approximately followed by the output phase noise of the reference input oscillator with a $20\log(N)$ difference. A peak appears at ω_n in the phase noise power spectral density where VCO noise is more dominant. So a large loop bandwidth is desired to reduce the phase noise of PLL due to VCO noise.

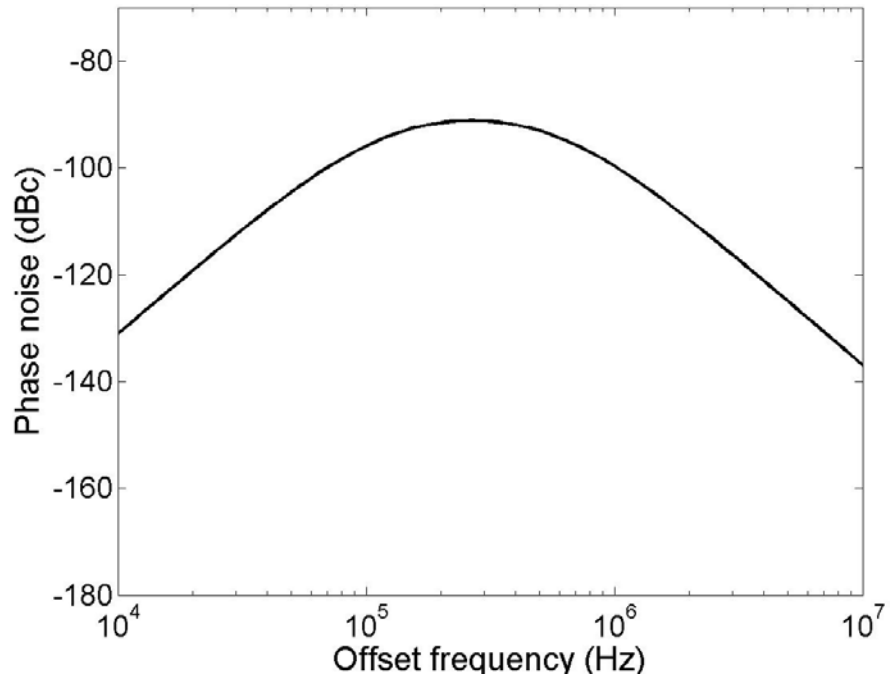


Figure 3.2: PLL phase noise for a noisy VCO and ideal input reference.

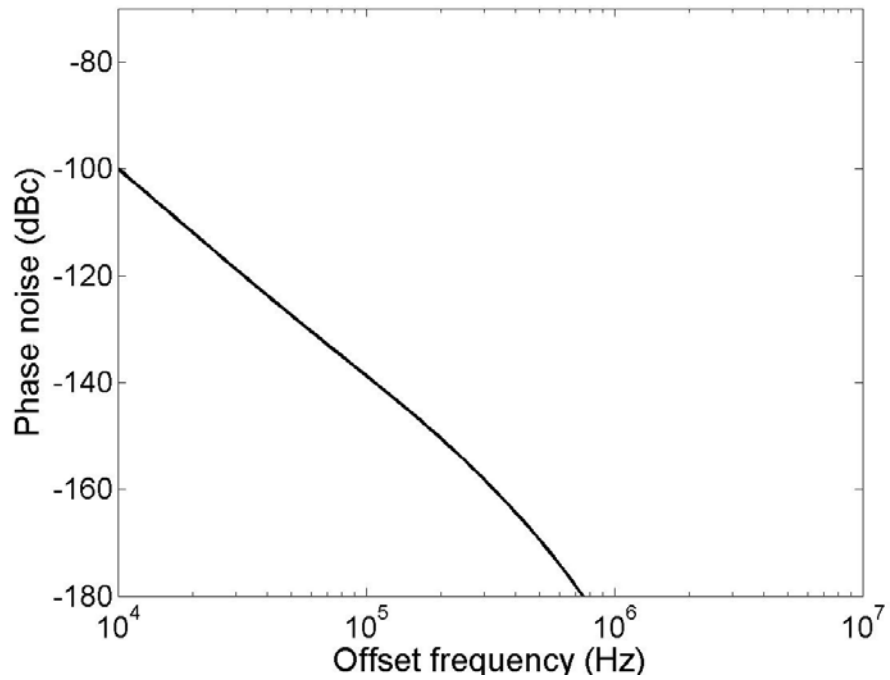


Figure 3.3: PLL phase noise for a noiseless VCO and noisy input reference.

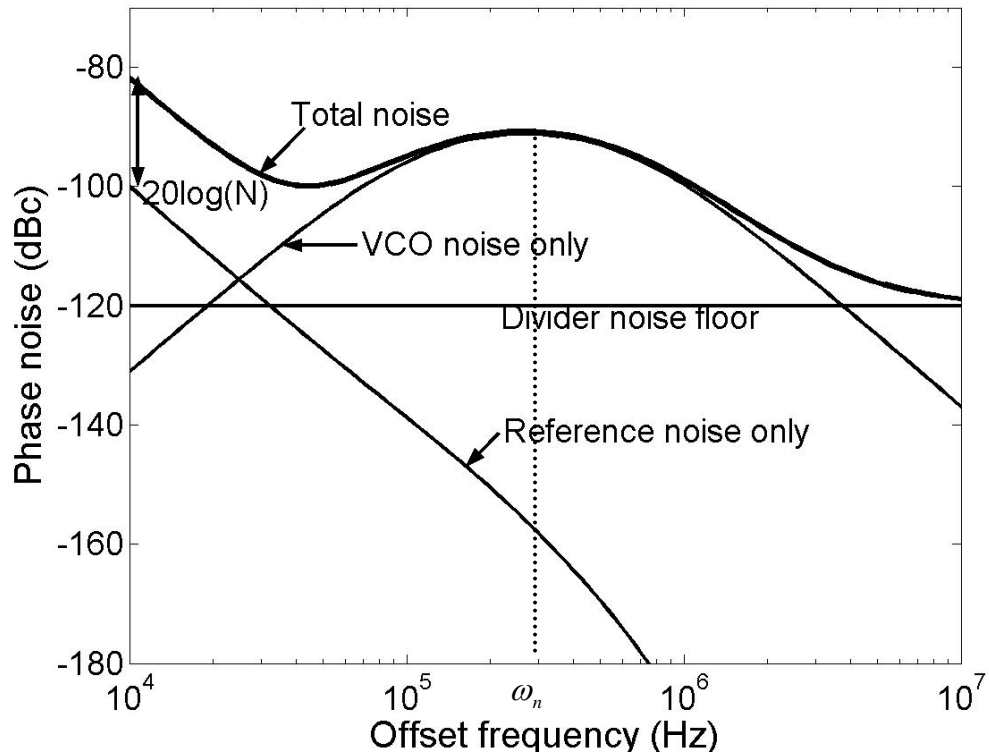


Figure 3.4: PLL phase noise with both noisy VCO and noisy input reference, considering the frequency divider noise floor.

3.3 Jitter Predication of PLL

For jitter analysis, again the input reference clock noise and the VCO noise are considered separately. The RMS jitter can be calculated by the phase noise power spectral density as shown in [43].

$$\sigma_{\Delta T}^2 = \frac{8}{\omega_0^2} \int_0^{\infty} S_{\Phi}(f) \sin^2(\pi f \Delta T) df \quad (3.7)$$

where ω_0 is the oscillation frequency, $S_{\Phi}(f)$ is the noise power spectral density and ΔT is the measurement interval. Equations (3.4) and (3.6) of power spectral density for VCO noise and input reference noise, respectively, can then be substituted into Eq. (3.7). The jitter expression for VCO noise only is approximately given by

$$\sigma_{VCO} = \frac{\sqrt{N_{VCO}}}{f_0} \cdot \sqrt{\frac{1}{2\zeta\omega_n}} \quad (3.8)$$

And the jitter expression for input reference noise only is approximately given by [43]

$$\sigma_{in} = \kappa \cdot \sqrt{\Delta T + \frac{1}{2\zeta\omega_n}} \quad (3.9)$$

where f_0 is the center frequency. $N_{VCO} = K_V^2 N_0 / 2$ characterizes the VCO output noise. κ is the jitter proportional constant for input reference noise. ΔT is the jitter measurement interval.

The total PLL long term RMS jitter shown in Fig. 3.5 can be computed using equation:

$$\sigma_{tot}^2 = \sigma_{in}^2 + \sigma_{VCO}^2 \quad (3.10)$$

Again the absolute value of the output jitter may change for different N_0 and κ values, which are highly dependent on applications, however the relative relationship between different noise sources and total jitter is shown clearly in Fig. 3.5. Here, for applications with comparable input noise and VCO noise, we assume that $\kappa^2 = 4\pi^2 N_0 / \omega^2$ in order to simplify the problem.

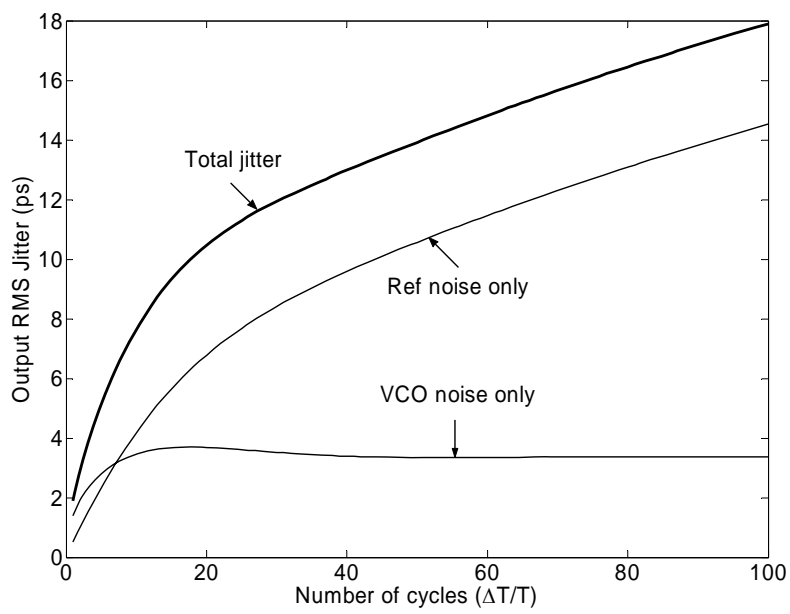


Figure 3.5: PLL output RMS jitter due to noisy VCO and noisy input reference.

3.4 Hot Carrier Effects on PLL

Hot carrier effects on VCOs have been studied in [29-31, 33]. VCO is an essential building block of PLL. The PLL tracking performance and phase noise degradation due to VCO performance degradation is presented in following sections. Hot carrier induced VCO gain degradation is focused in this work. Then the impact of VCO gain degradation on PLL performance is investigated in the following sections.

3.4.1 Hot Carrier Induced Degradation on VCO Gain

CMOS VCO circuit performance is definitely affected by hot-carrier effects. The gain of VCO, K_V , is a very important parameter when dealing with the PLL tracking, and phase noise and jitter performance. A model of VCO gain decrease due to the degradation on n-MOSFET parameters is shown in [29]. Degradations of device parameters include increase in threshold voltage and decrease in electron mobility. In this work, a more detailed analysis of a simple but very widely used VCO, current starved VCO, is presented. Most of the ring oscillator based VCO [11, 29] have the similar frequency adjusting mechanism as a current starved VCO. The biasing current is varied by adjusting the control voltage, so that the time it takes to charge and discharge the equivalent load capacitance of each stage is varied. As a result, the output frequency is adjusted by the control voltage. It is beneficial to study the performance degradation of a current starved VCO.

A current starved VCO under consideration is shown in Fig. 3.6. Assuming the biasing current is satisfied by the square law relation with the control voltage, V_{CTRL} . The oscillation is achieved by charging and discharging the equivalent capacitance, C_L , in each stage of the VCO.

The oscillation frequency of the current starved VCO for n (an odd number ≥ 3) of stages is given by

$$f_o = \frac{1}{n(t_r + t_f)} \approx \frac{I_D}{n \cdot C_L \cdot V_{DD}} \quad (3.11)$$

where t_r and t_f are the rising time and the fall time, respectively. V_{DD} is the power supply voltage. I_D the drain current of M4, which is the exact biasing current of M2 and M3. I_D is not equal to total biasing current I_{BIAS} , because the M4 may operate out of the saturation region. However, in the small linear tuning range of V_{CTRL} , I_D and I_{BIAS} are approximately considered to be same.

The characteristic of the oscillation frequency versus the control voltage should be linear in order to keep the gain of VCO, K_V , as a constant value. The useful VCO operation range should be this linear range, where f_o is linearly depend on V_{CTRL} . This linear range is typically small in a current starved VCO.

The simulated characteristic of f_o versus V_{CTRL} is shown in Fig. 3.7. It shows the linear range of V_{CTRL} from 0.7 V to 1.1 V, while f_o lies in the range of 240 MHz to 870 MHz, which leads to a VCO gain of 1575 MHz/V.

The drain current of M1 can be approximately given by the saturation expression

$$I_D = \frac{1}{2} \cdot \mu \cdot C_{OX}' \cdot \frac{W}{L} \cdot (V_{CTRL} - V_{th})^2 \quad (3.12)$$

So, the gain of VCO, K_V , can be given by

$$K_V = \frac{\partial f_o}{\partial V_{CTRL}} = \frac{\mu \cdot C_{OX}' \cdot W \cdot (V_{CTRL} - V_{th})}{n \cdot L \cdot C_L \cdot V_{DD}} \quad (3.13)$$

or by considering the transconductance of M1, G_m , Equation (3.13) can be written as

$$K_V = \frac{\partial f_o}{\partial V_{CTRL}} = \frac{G_m}{n \cdot C_L \cdot V_{DD}} \quad (3.14)$$

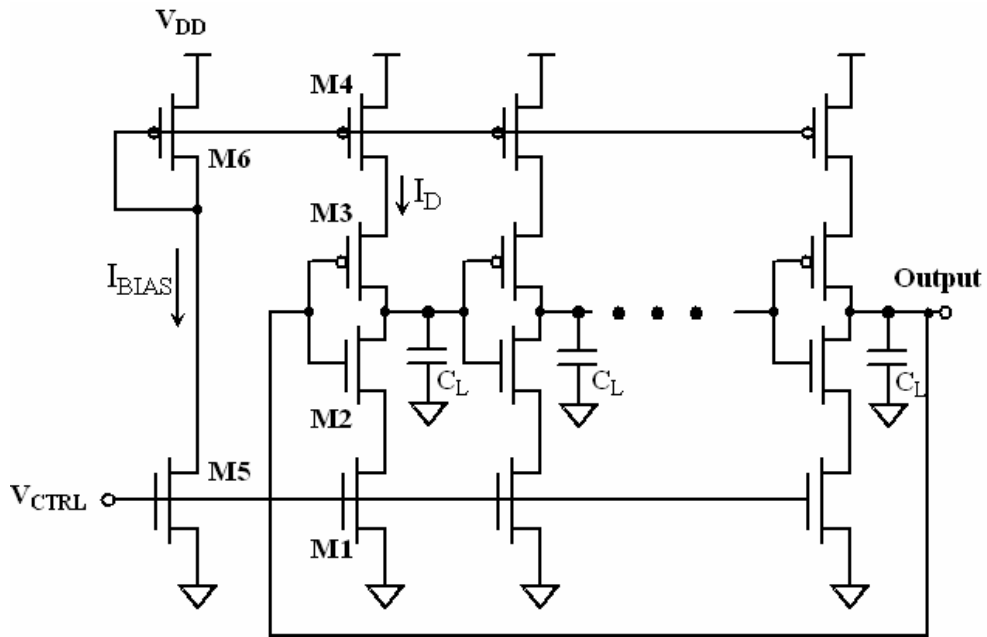


Figure 3.6: A current starved VCO with equivalent load capacitances.

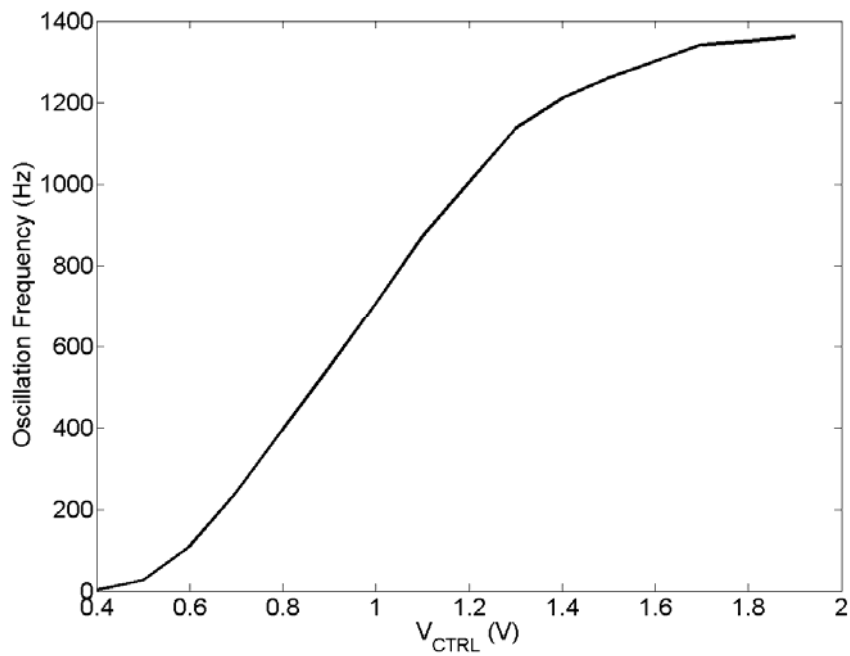


Figure 3.7: The simulated characteristic of f_o versus V_{CTRL} .

It is shown in Eq. (3.13) that K_v is a function of threshold voltage, V_{th} and mobility, μ . Moreover, Eq. (3.14) shows K_v can also be described as a function of the device transconductance, G_m . These parameters can be degraded due to the hot-carrier effect. The model of VCO gain can be modified for hot carrier consideration.

Considering the hot-carrier degradation in changing threshold voltage and mobility, the degradation of VCO gain can be given by

$$K'_v = \frac{(\mu - \Delta\mu) \cdot C'_{OX} \cdot W \cdot (V_{CTRL} - V_{th} - \Delta V_{th})}{n \cdot L \cdot C_L \cdot V_{DD}} \quad (3.15)$$

$$\frac{\Delta K_v}{K_v} = 1 - \left(1 - \frac{\Delta\mu}{\mu}\right) \left(1 - \frac{\Delta V_{th}}{V_{CTRL} - V_{th}}\right) \quad (3.16)$$

Considering the degradation in transconductance, the degradation of VCO gain can be given by

$$\frac{\Delta K_v}{K_v} = \frac{\Delta G_m}{G_m} \quad (3.17)$$

The degradation in transconductance can be described as combining the effects of change in threshold voltage and mobility. Simulated VCO tuning characteristic before and after stress is shown in Fig. 3.8. Figure 3.9 shows the VCO gain degradation versus the hot-carrier stress time.

To investigate the VCO gain degradation due to hot-carrier effects, a fixed oscillation frequency is necessary to make the analysis more applicable. Assuming the VCO operates at 800 MHz center frequency, the VCO gain changes from 1575 MHz/V to 940 MHz/V before and after the hot-carrier stress.

Simulation based on experimental results shows if threshold voltage increases by 40% and the mobility decreases by 45% after 4 hours of stress, K_v can decrease by 40% [29]. Note that due to hot-carrier effect the control voltage is shifted to keep a fixed oscillation frequency. This may also cause severe problem in PLL tracking ability.

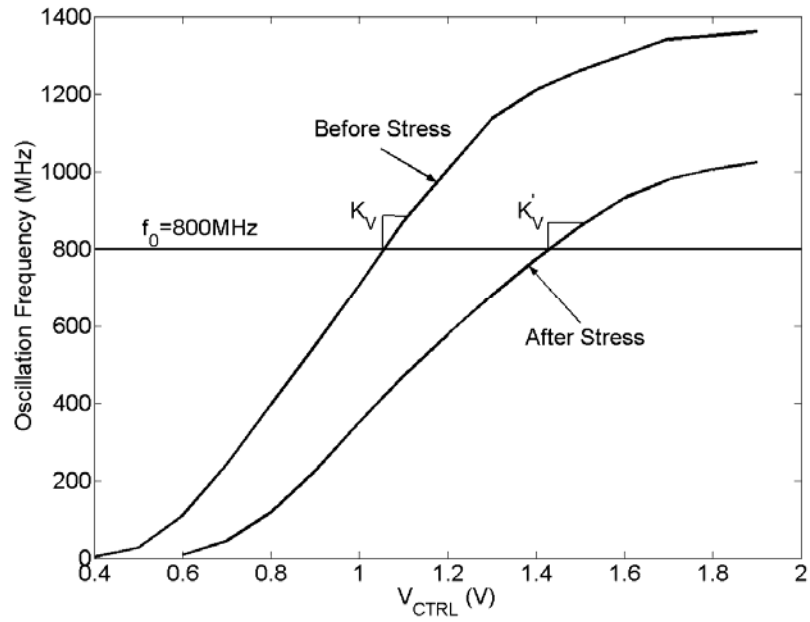


Figure 3.8: Simulated VCO tuning characteristic before and after stress.

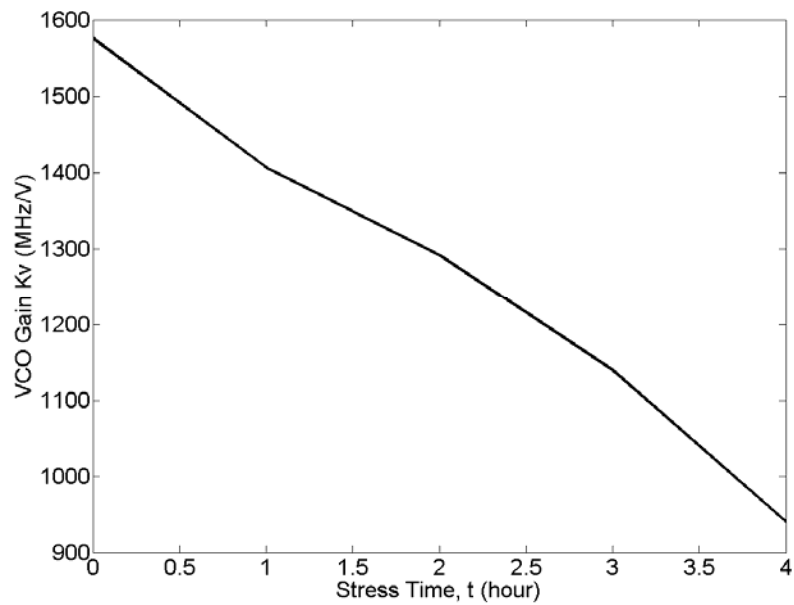


Figure 3.9: VCO gain degradation versus stress time at 800 MHz oscillation frequency.

3.4.2 Hot Carrier Induced Degradation in PLL Loop Dynamics

The loop bandwidth and damping factor characterize the closed-loop response. In general, ω_n determines the cut-off frequency of the response and ζ determines the shape of the characteristic. PLL is critically damped with a damping factor of one and over damped with damping factors greater than one. Equations (3.18) and (3.19) give the expressions for the loop bandwidth and the damping factor with K_v as a parameter [41]:

$$\omega_n = \frac{2 \cdot \zeta}{R \cdot C_1} = \sqrt{\frac{K_v I_{CH}}{N C_1}} \quad (3.18)$$

$$\zeta = \frac{1}{2} \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_v \cdot R^2 \cdot C_1} \quad (3.19)$$

All parameters remain constant except K_v under hot-carrier effect. The hot-carrier induced degradation on VCO gain K_v will cause the degradation on the loop parameters ζ and ω_n . The relationship describing shift in parameters is given by

$$\frac{\Delta \zeta}{\zeta} \text{ (or } \frac{\Delta \omega_n}{\omega_n}) = 1 - \sqrt{1 - \frac{\Delta K_v}{K_v}} \quad (3.20)$$

When there is a 40% decrease of K_v , the loop bandwidth and damping factor will decrease by about 23%. The hot-carrier induced degradation on loop dynamics can be seen from frequency response and step response characteristics, shown in Figs. 3.10 and 3.11, respectively. As shown in these figures, after stress loop bandwidth decreases, and the time it takes to track the step input increases.

3.4.3 Hot Carrier Effects on Phase Noise in PLL

The phase noise properties in PLL are functions of loop bandwidth, which is a function of VCO gain, K_v . Therefore the hot-carrier induced degradation on VCO gain may cause the phase

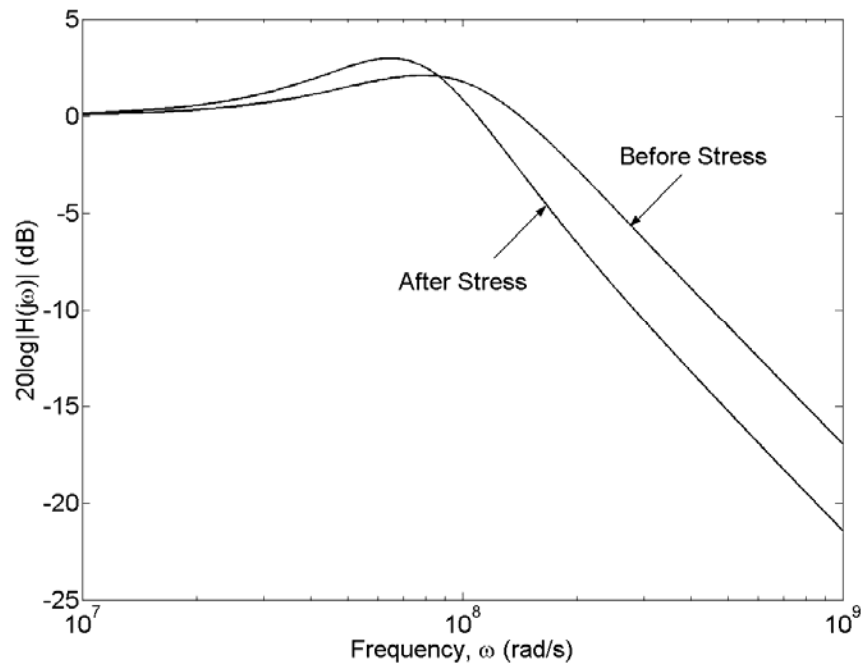


Figure 3.10: Frequency response of PLL change due to hot-carrier effect.

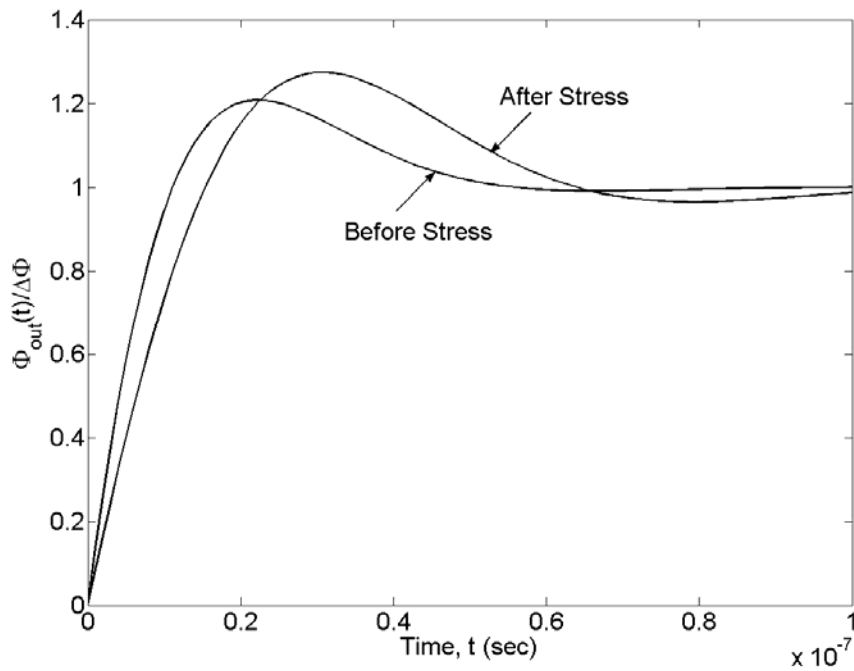


Figure 3.11: Step response of PLL change due to hot-carrier effect.

noise properties change in PLL. For a center frequency of 800 MHz and loop bandwidth of 16 MHz PLL, after using the graphical treatment on the input reference noise, the VCO noise and the frequency divider noise, the total phase noise degradation due to hot carrier stress is shown in Fig. 3.12, considering the noise contribution of the frequency divider. Combining the degradation on noisy VCO and noisy input reference, the total degradation can be noticed by an increase in phase noise at lower offset frequency and a left-shifting peak of phase noise power spectral density.

3.4.4 Hot-Carrier Effects on Jitter in PLL

The output jitter properties of PLL are also functions of loop parameters including loop bandwidth and damping factor, which in turn are related to the VCO gain, K_V . Therefore, the hot-carrier induced degradation on VCO gain also causes the jitter properties change in PLL. After using the jitter graphical treatment, the RMS jitter degradation due to hot carrier stress is shown in Fig. 3.13. The most significant degradation on jitter performance occurs when the measurement interval is around 35 clock cycles, which gives a 17% increase in total output RMS jitter.

3.5 Summary

In this work, an attempt has been made to develop phase noise and jitter predication method for a second order PLL. Then hot carrier induced degradation on single-ended current starved VCO gain is studied.

Analytical results of hot carrier effects on tracking performance, phase noise and jitter in PLL circuit designed in 0.25 μm N-well CMOS process are presented. The analytical models which take into consideration hot carrier effects have shown that after four hours of stress, the gain of a current-starved VCO degrades from 1575 MHz/V to 940 MHz/V, which is about a 40% decrease in gain at an oscillation frequency of 800 MHz.

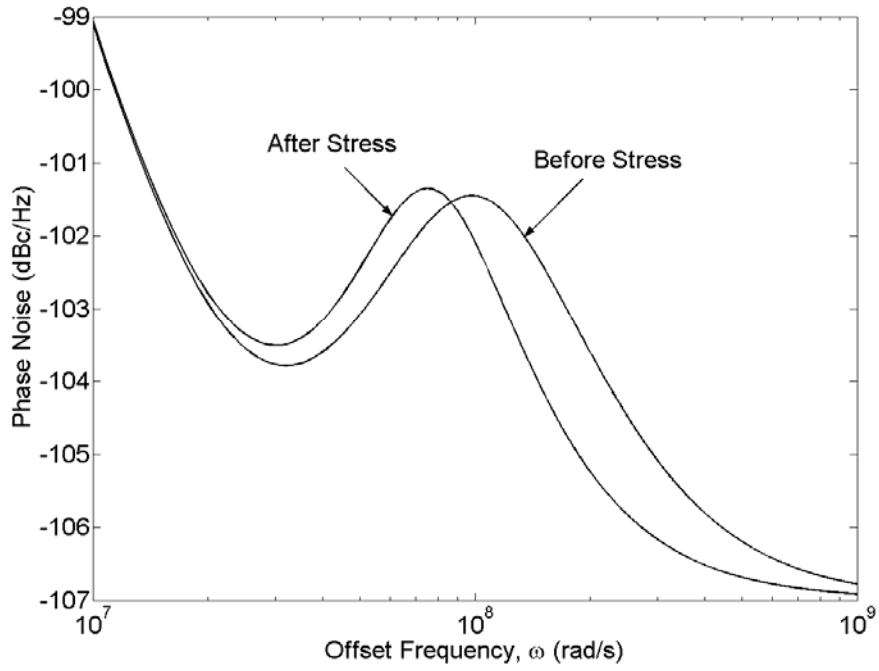


Figure 3.12: Hot carrier induced degradation on phase noise performance.

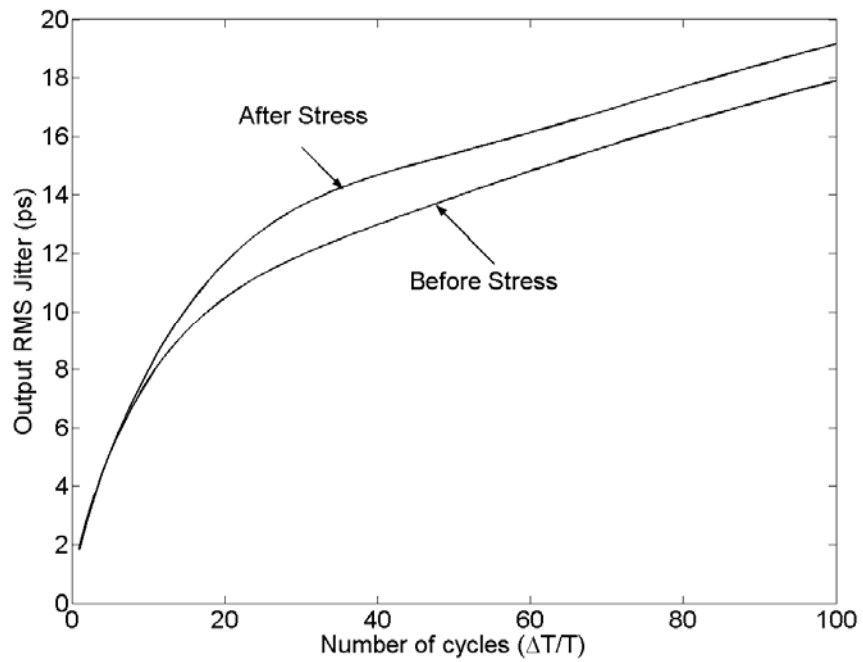


Figure 3.13: Degradation on output RMS jitter change due to hot-carrier effect.

The loop dynamics, phase noise and output clock jitter of a second order PLL are studied using s-domain analysis for a feedback control system. The degradation on PLL loop parameters and noise properties are analyzed for a second order PLL with a center frequency of 800 MHz, loop bandwidth of 16 MHz. The loop parameters, i.e., the loop bandwidth frequency and damping factor decrease by about 23% after stress, which in turn decrease the loop bandwidth and increase the tracking time, respectively. The degradation causes a noticeable increase in phase noise at a lower offset frequency, 1 dB increase at 8 MHz offset, and a left-shifting peak of phase noise power spectral density.

Hot carrier induced degradation on VCO gain also influences the jitter properties of PLL. The most significant degradation occurs when the measurement interval is around 35 clock cycles, which gives about 17% increase in total output RMS jitter. And there is around 15% increase in long term RMS jitter.

CHAPTER 4[‡]

AN EXPERIMENTAL STUDY OF PHASE NOISE IN CMOS PHASE-LOCKED LOOPS

The loop model of a second order phase-locked loop (PLL) is presented in Chapter 3. The effects of different building blocks on the phase noise performance of PLLs are analyzed. Input reference clock, voltage-controlled oscillator (VCO) and the frequency divider are the dominant noise sources in a PLL system. PLL phase noise prediction by the graphical treatment is also introduced. In this chapter, an experimental study of phase noise on PLL is carried out. Simulation and experimental measurement results of the phase noise are reported on a single-ended current-starved VCO, a double-ended differential VCO. Moreover, two PLLs are designed and fabricated with same input reference clock and frequency divider but different VCO structures. Two types of VCOs have different gain and output noise properties. This allows us to verify the PLL phase noise graphical treatment method given in the previous Chapter 3 based on different PLL designs. Experimental results closely follow the predicted performance which is obtained by the graphical treatment.

4.1 Proposed PLL Circuits Design

Two PLL chips have been designed based on different VCO structures. Open loop VCOs are also included to study the open loop VCO phase noise. All circuits are designed and fabricated using $0.5\ \mu\text{m}$ n-well CMOS technology. The only difference of two PLL chips is the VCO structure. Designed loop parameters are same in two different PLLs. The loop parameters are as follows: $N = 8$, $I_{CH} = 30\ \mu\text{A}$, $R = 41.5\ \text{k}\Omega$, $C_1 = 43.3\ \text{pF}$ and $C_2 = 100\ \text{fF}$. The only

[‡] Part of this work is reported in following publications:

1. C. Zhang, A. Srivastava and C. Ni, "An experimental study on phase noise in phase-locked loops considering different noise sources," *Proc. of 49th IEEE International Midwest Symposium on Circuits and Systems*, August 6-9, 2006. Selected as one of the 12 finalists in Student Paper Contest (SPC).
2. C. Zhang, A. Srivastava and C. Ni, "An experimental study on phase noise in phase-locked loops considering different noise sources," *Analog Integrated Circuits and Signal Processing*, 2006 (under review).

parameter which is different in these two PLLs is the VCO gain. Therefore, for different VCO gain, different PLL output noise properties can be observed.

4.1.1 Phase Frequency Detector

The phase frequency detector (PFD) used in this design is a conventional one except some inverters are added to adjust the delay so that the spurs at the output can be reduced. The circuit diagram of the PFD is shown in Fig. 4.1. The simulated PFD output due to input phase difference is shown in Fig. 4.2. The simulated result shows the frequency of the input reference clock is lower than the VCO clock and the phase of the VCO clock is leading which result in a positive average ‘dn’ signal. This PFD is suitable for less than 100 MHz input signals. For higher frequency operation, some new structures have to be used which will be discussed in the following chapter.

4.1.2 Charge Pump

A typical current mirror structure is used for the charge pump design. Figure 4.3 shows the circuit diagram of the charge pump. The charge pump current I_{CH} is designed to be $30\mu A$. The width ratio between two mirror branches gives the current ratio. Mp and Mn serve as the switch MOSFETs switched by ‘upn’ and ‘dn’ signal generated from the PFD, controlling the charge/discharge path of the charge pump.

4.1.3 Frequency Divider

The circuit diagram of the frequency divider is shown in Fig. 4.4. A D-flipflop and an inverter loop form a divide-by-two stage. The divide-by-eight divider consists of three divide-by-two stages. Similarly with PFD, this divider circuit is only suitable for clock frequency in MHz range. For GHz range frequency operation, a dynamic frequency divider has to be used which will be discussed in the following chapter.

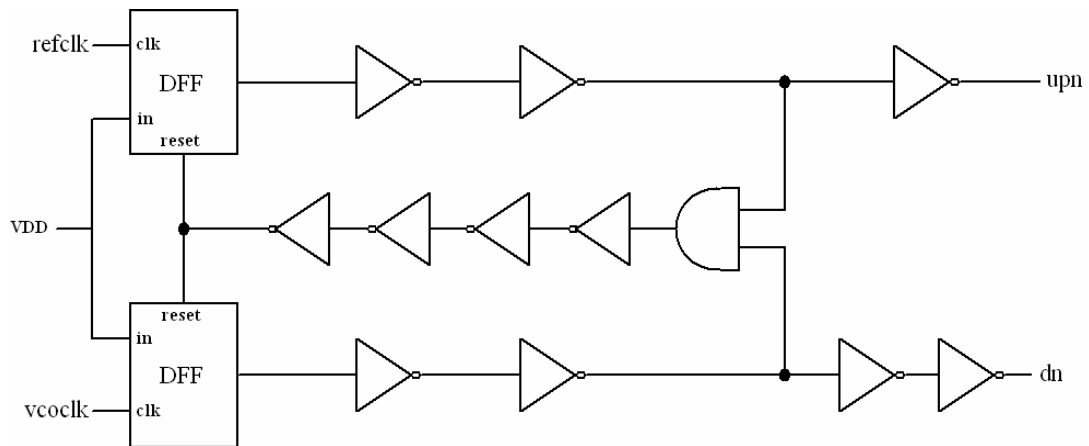


Figure 4.1: Circuit diagram of the phase frequency detector (PFD).

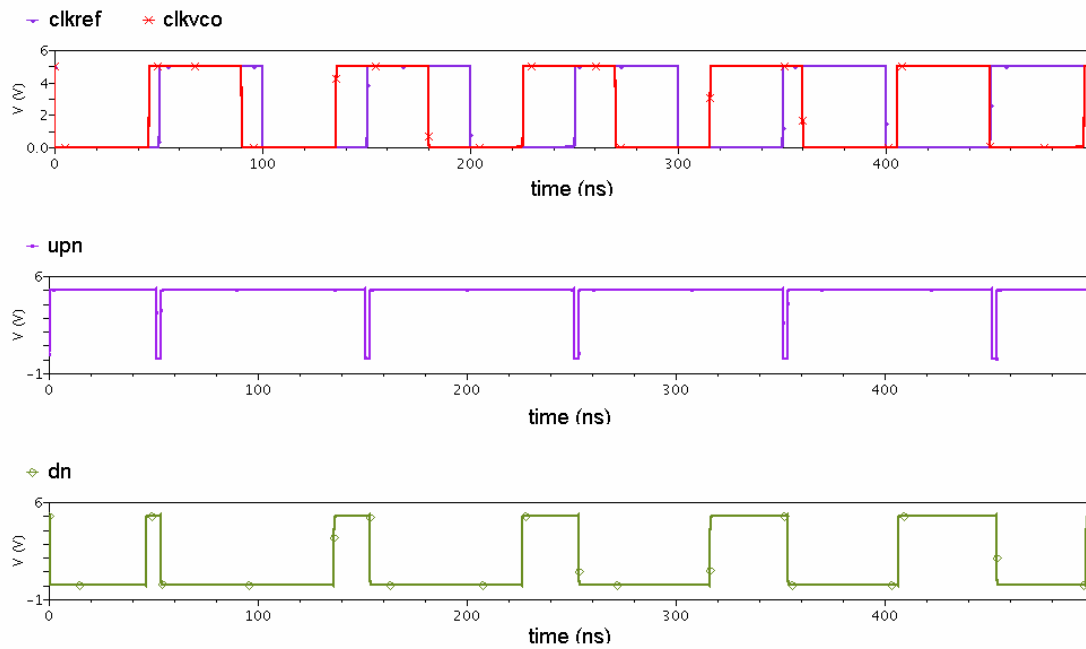


Figure 4.2: Simulated results of the PFD outputs due to different input phase (reference clock phase is leading the VCO output clock phase).

4.1.4 Voltage-Controlled Oscillator

Two types of VCOs are designed. These are a single-ended current starved VCO and a double-ended differential VCO. The current-starved VCO is conventional compared to the differential one which has been shown in previous chapter. The differential VCO circuit is shown in Fig. 4.5. There is an auxiliary biasing circuit block in the differential VCO, shown in Fig. 4.6 in order to reduce the differential VCO gain and achieve a more linear frequency – voltage tuning characteristic. The resistor (20 k Ω) connects the two branches of a current mirror to balance the current difference. The current in the mirror branch changes linearly with the control voltage and changes slower than the circuit without the balance resistor. It decreases the VCO gain.

4.2 Phase Noise Simulation and Measurement Results

In this section, PLL phase noise predicted results and experimental results on two different PLLs are presented. The prediction is done by the graphical treatment method, and the phase noise measurement is conducted using a spectrum analyzer. The prediction method is recalled and the measurement setup is presented.

Recall the phase noise analysis of PLL in Chapter 3. For an open loop VCO, the output noise spectrum can be approximated from Eq. (3.1) after neglecting the ω_{1/f^3} term for input flicker noise and N_1 term for output thermal noise, and is given by

$$S_{\Phi_{out}}(\omega) = \frac{2\pi^2 K_V^2 N_0}{\omega^2} \quad (4.1)$$

If we know the VCO output phase noise profile, the term $N_0/2$ can be easily determined through this equation. $N_0/2$ characterizes the double-side band power spectral density of the

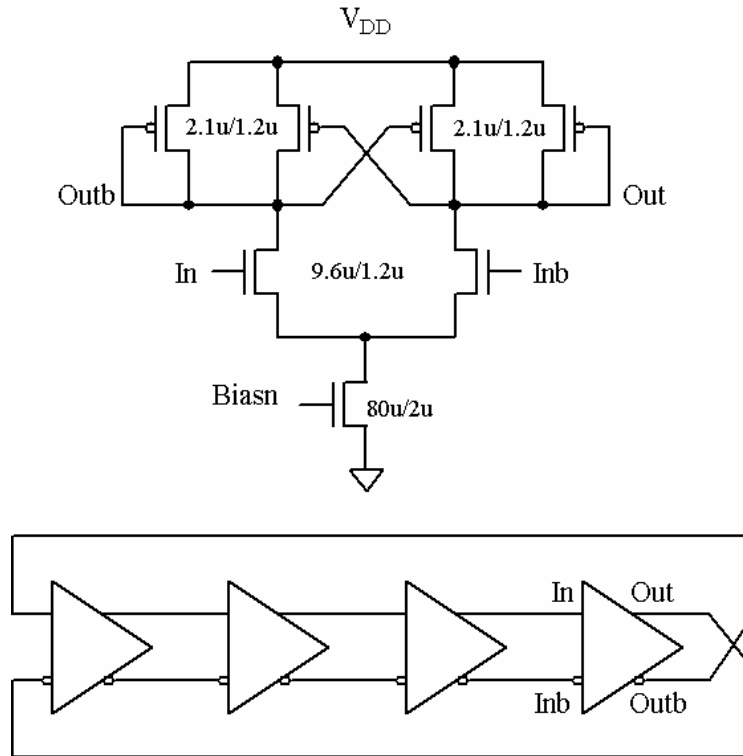


Figure 4.5: Circuit diagram of the double-ended differential VCO.

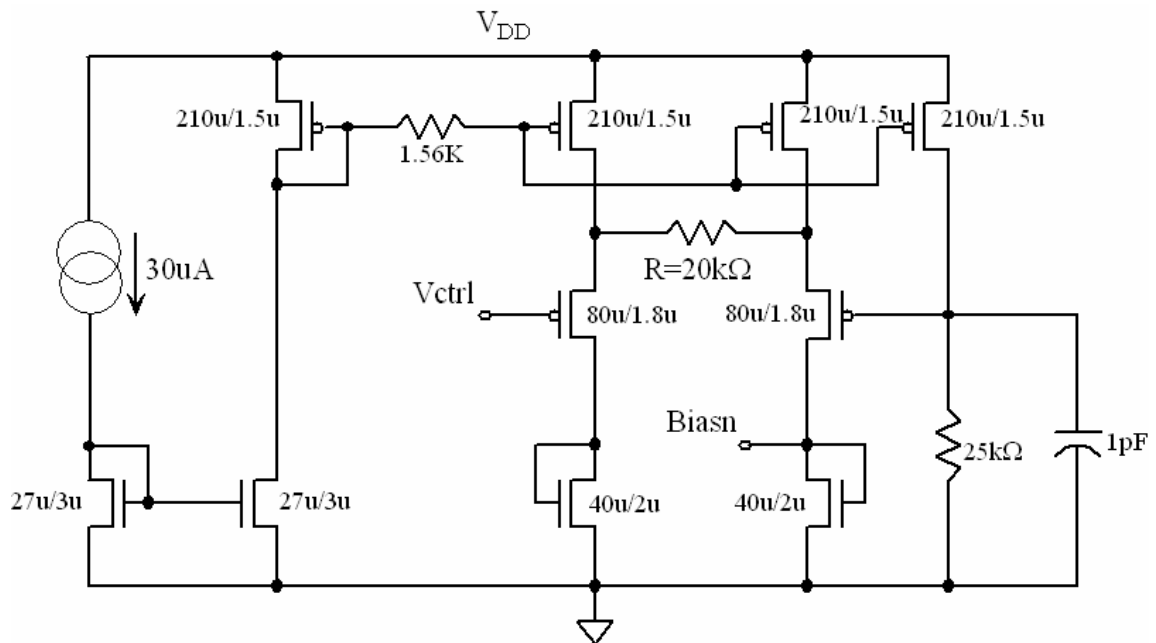


Figure 4.6: The double-ended differential VCO biasing circuit.

input white noise of VCO. Moreover, for a PLL, the phase noise model due to VCO noise and input reference noise are given by Eqs (3.4) and (3.6), and reproduced below as Eqs. (4.2) and (4.3), respectively.

$$S_{\Phi_{out}}(\omega) = \frac{N_0}{2} \cdot \frac{4\pi^2 C_1^2 N^2}{I_{CH}^2} \cdot \frac{\omega^2}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \omega^2 \tau^2} \quad (4.2)$$

$$S_{\Phi_{out}}(\omega) = \frac{\alpha}{\omega^2} \cdot \frac{\omega^2 \tau^2 + 1}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \omega^2 \tau^2} \quad (4.3)$$

The term α in Eq. (4.3) can be determined by the input clock which is a function generator, Agilent 33220A in this work. VCO gain K_V can be measured from the open loop VCO. The loop bandwidth ω_n can be calculated by $\omega_n = \sqrt{(K_V I_{CH}) / (N C_1)}$. The loop filter time constant $\tau = R C_1$. Since, all the parameters in Eqs. (4.2) and (4.3) are known, the $20\log(N)$ phase noise and the noise floor introduced by the frequency divider are considered, by means of the superposition we can get the predicted PLL phase noise curve.

VCO gain measurements have been done on two different VCOs. VCO tuning characteristics are shown in Fig. 4.7. The gain of the differential VCO is 30 MHz/V while for the single-ended VCO it is 90 MHz/V. Therefore, the loop bandwidths are 267 kHz and 462 kHz for PLL with differential VCO and single-ended VCO, respectively. All the input reference clocks are generated using a single function generator, so that the parameter α can be properly chosen to characterize its output noise property.

Phase noise measurements are conducted by a spectrum analyzer Agilent 8561EC. The spectrum of the clock signal from differential VCO is observed. The powers of spectrum on each

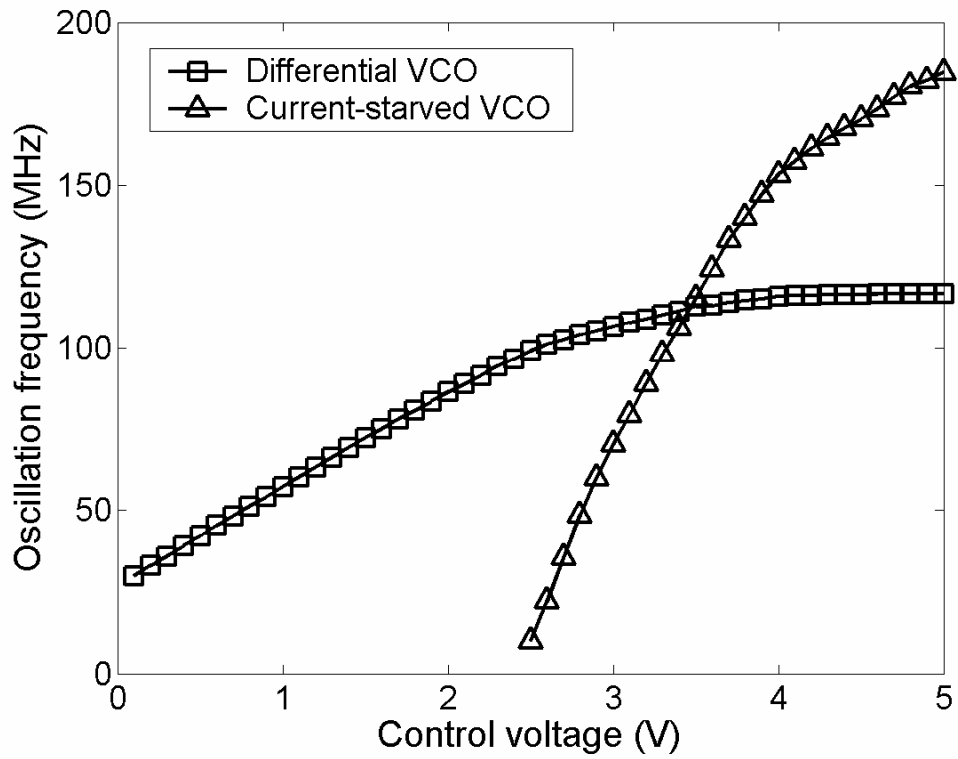


Figure 4.7: The tuning characteristics for differential and current-starved VCO.

offset frequencies are recorded. The result is then converted to phase noise power spectrum density curve using Eq. (1.1).

The simulation and experimental results of phase noise at different center frequencies for differential VCO are shown in Fig. 4.8 and results for single-ended VCO are shown in Fig. 4.9. Given the output noise pattern of the open loop VCO, the parameter $N_0/2$ can be set from Eq. (4.1) and substituted in Eq. (4.2), and then the simulated PLL output phase noise can be achieved using the superposition method.

The PLL phase noise simulation and measurement results for different VCO and different center frequencies are shown in Figs. 4.10 and 4.11, respectively. The curve with solid line is the simulated PLL phase noise which is obtained by the superposition of the simulated phase noise curve caused by VCO noise, input reference noise and the frequency divider noise. The peak of the solid line characterizes the loop bandwidth. As seen in Figs. 4.10 to 4.13, PLL with differential VCO has a smaller bandwidth compared to PLL with single-ended VCO. Moreover, the magnitude of the peak characterizes the parameter $N_0/2$, which is larger for the smaller center frequency for both VCOs. This difference can be also noticed in the open loop VCO output phase noise curve for different center frequencies as shown in Fig. 4.8 and 4.9. Evaluated $N_0/2$ values for differential VCO are $3 \times 10^{-16} V^2 / Hz$ and $9 \times 10^{-16} V^2 / Hz$ for 100 MHz and 80 MHz oscillation frequency, respectively. And for single-ended VCO the values are $9 \times 10^{-16} V^2 / Hz$ and $9 \times 10^{-15} V^2 / Hz$ for 100 MHz and 80 MHz oscillation frequency, respectively.

The triangle markers in Figs. 4.10 to 4.13 represent the measured phase noise at particular offset frequencies. As seen in Figs. 4.10 and 4.11, for the PLL with differential VCO,

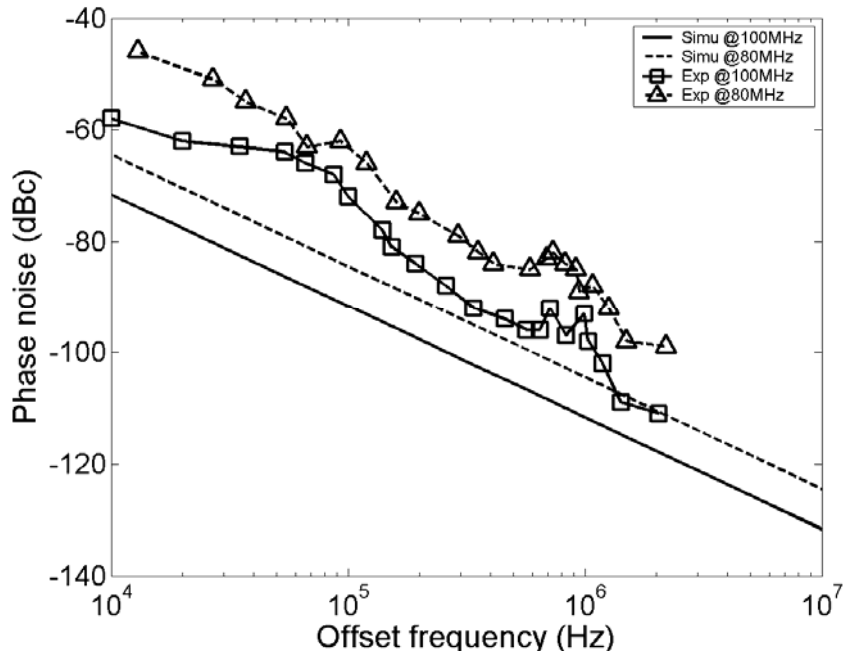


Figure 4.8: Simulation and experimental results of the open loop VCO output phase noise at 100 MHz and 80 MHz center frequency for differential VCO.

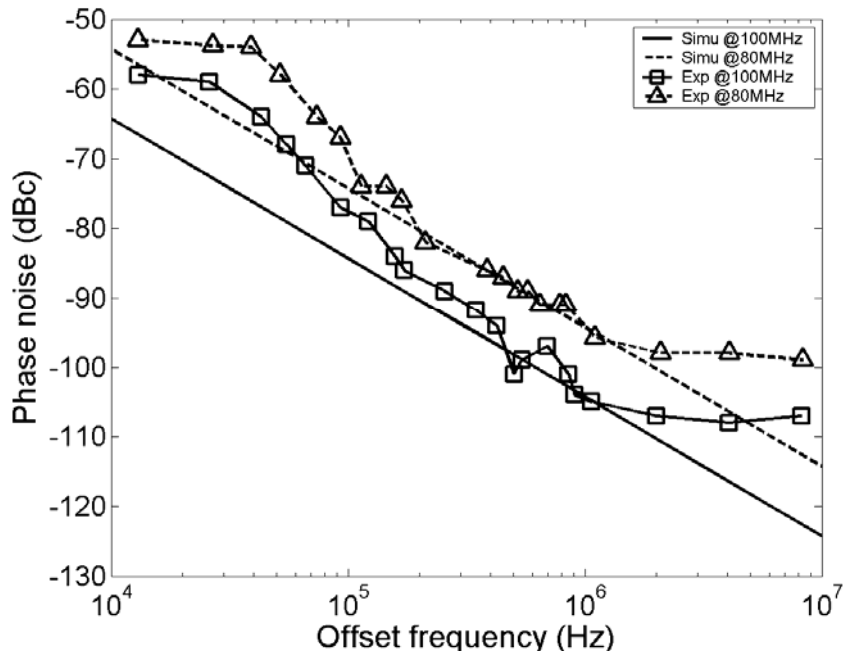


Figure 4.9: Simulation and experimental results of the open loop VCO output phase noise at 100 MHz and 80 MHz center frequency for single-ended VCO.

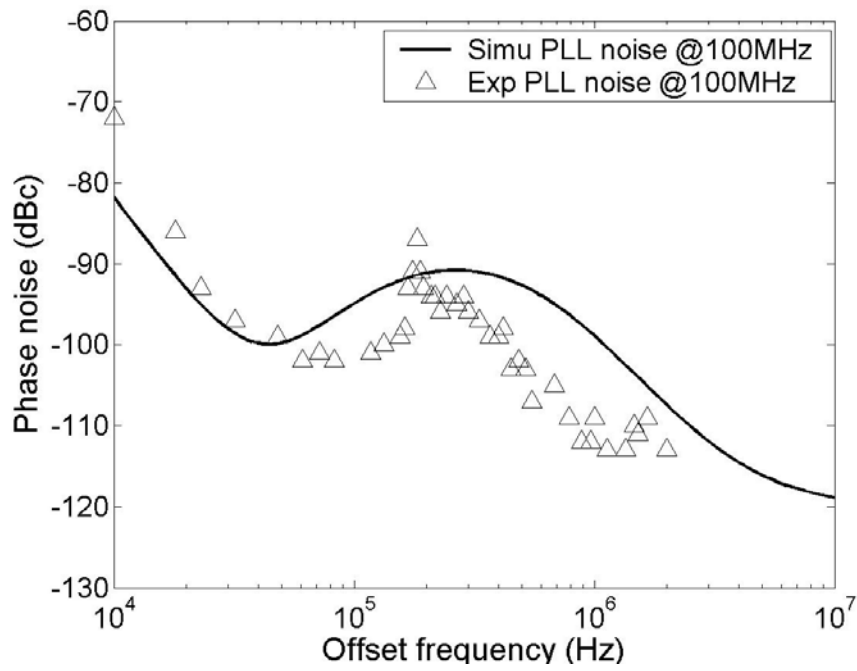


Figure 4.10: Simulation and experimental results of PLL phase noise at 100 MHz center frequency for differential VCO.

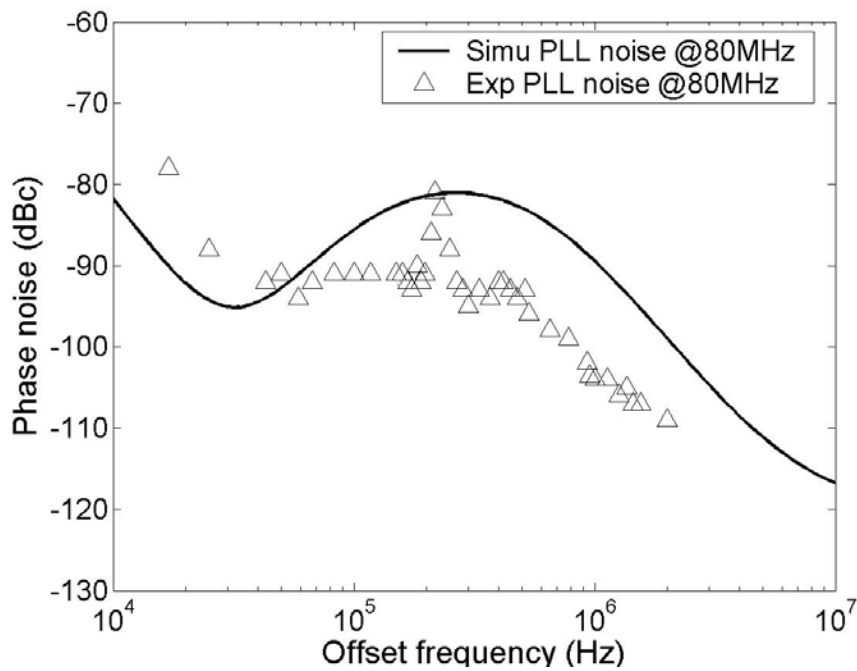


Figure 4.11: Simulation and experimental results of PLL phase noise at 80 MHz center frequency for differential VCO.

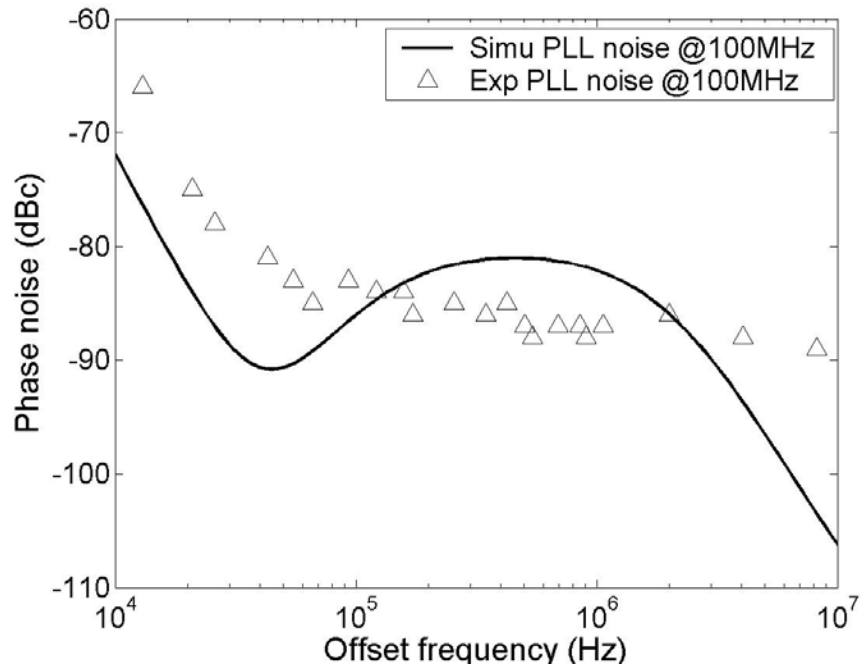


Figure 4.12: Simulation and experimental results of PLL phase noise at 100 MHz center frequency for single-ended VCO.

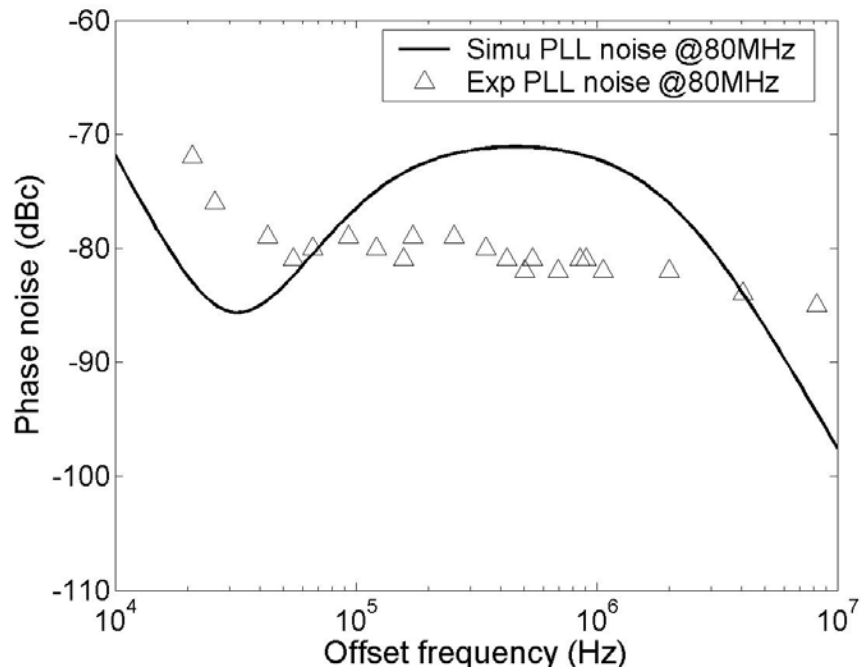


Figure 4.13: Simulation and experimental results of PLL phase noise at 80 MHz center frequency for single-ended VCO.

the measured output phase noise has a peak near the predicted loop bandwidth of 267 kHz. Although the peak is narrower than the predicted curve, it follows the predicted noise behavior and clearly points that the phase noise superposition treatment is suitable to predict the PLL output phase noise. On the other hand, for the PLL with single-ended VCO which has larger bandwidth, there is no peak observed in phase noise curves in Figs. 4.12 and 4.13. The measured phase noise data flatten out at the predicted peak position, i.e. 462 kHz, however, the measured behavior follows the predicted PLL noise performance. For the single-ended VCO, the simulation results show a large change at the phase noise peak position compared to the differential VCO. This may be explained by their different bandwidths. A PLL with larger bandwidth is more subject to input reference clock noise than the VCO noise. In other words, a larger bandwidth is suitable to suppress the VCO noise. In our work, the PLL with single-ended VCO has a large bandwidth than the PLL with differential VCO. As described in Chapter 3, the peak in the phase noise profile is dominated by the VCO noise. If the VCO noise is suppressed by the larger bandwidth, the peaking in phase noise profile is somehow vanished. This explains that the phase noise profile flattens out for the PLL with single-ended VCO which has a large bandwidth and is less affected by the VCO noise.

4.3 Summary

It is shown that the building blocks of a PLL contribute to its overall output noise which can be predicted by the graphical treatment of each noise source. The important noise sources are input reference clock, VCO and the frequency divider. Different PLLs with different VCOs have been fabricated in $0.5\ \mu\text{m}$ CMOS technology. For the PLL with differential VCO, the measured output phase noise has a peak near the predicted loop bandwidth of 267 kHz. It follows the predicted noise behavior though the peak is narrower than the predicted curve. On the other hand, for the PLL with single-ended VCO which has larger bandwidth, there is no peak observed

in phase noise curves. The measured phase noise data flatten out at the predicted peak position, i.e. 462 kHz; however, the measured behavior follows the predicted PLL noise performance. Commercial tools for PLL phase noise simulation are not available. This work provides a very useful tool to predict PLL phase noise at the circuit design level.

CHAPTER 5[§]

PHASE NOISE AND JITTER ANALYSIS OF AN ADAPTIVE BANDWIDTH LC-VCO BASED PHASE-LOCKED LOOP

This chapter investigates the phase noise and timing jitter performance parameters of an adaptive bandwidth LC-VCO based Phase-Locked Loop (PLL). Recent studies [43, 44] have explored jitter performance in the light of optimization of PLL loop parameters. Adaptive bandwidth PLL structures have been discussed at length in [44-46]. However, no detailed study for phase noise and jitter optimization on PLL with tunable loop parameters has been reported in the literature. This work attempts to study the noise performance of an adaptive bandwidth LC-VCO based PLL. The 3 GHz adaptive bandwidth PLL incorporating an LC-VCO structure is designed in a 0.25 μm *N*-well CMOS process. A charge pump in conjunction with a tuneable loop filter facilitates the adaptive bandwidth feature. Simulation results demonstrate the impact on phase noise and jitter performance with variations in the loop parameters. Moreover, the impact of quality factor (Q) of the on-chip spiral inductor on phase noise and jitter performance of the proposed PLL is also investigated.

5.1 Proposed Adaptive Bandwidth PLL Design

A 3 GHz adaptive bandwidth PLL with an LC-VCO is designed in a 0.25 μm *N*-well CMOS process. Adjustable charge pump and loop filter components are designed with the adaptive bandwidth feature in mind. The block diagram of the PLL circuit is shown in Fig. 5.1. Eqs. (1.10) and (1.11) demonstrate that the PLL loop parameters, damping factor and loop bandwidth can be adjusted by controlling the charge pump current, I_{CH} , or the loop filter resistor,

[§] Part of this work is reported in following publication:

C. Salimath, C. Zhang and A. Srivastava, "Impact of Q-factor of an on-chip integrated inductor on the phase noise performance of a CMOS LC VCO based phase-locked loops," *The 7th Louisiana Materials and Emerging Technologies Conference*, Louisiana State University, Baton Rouge, October 23-24, 2006 (Poster Paper).

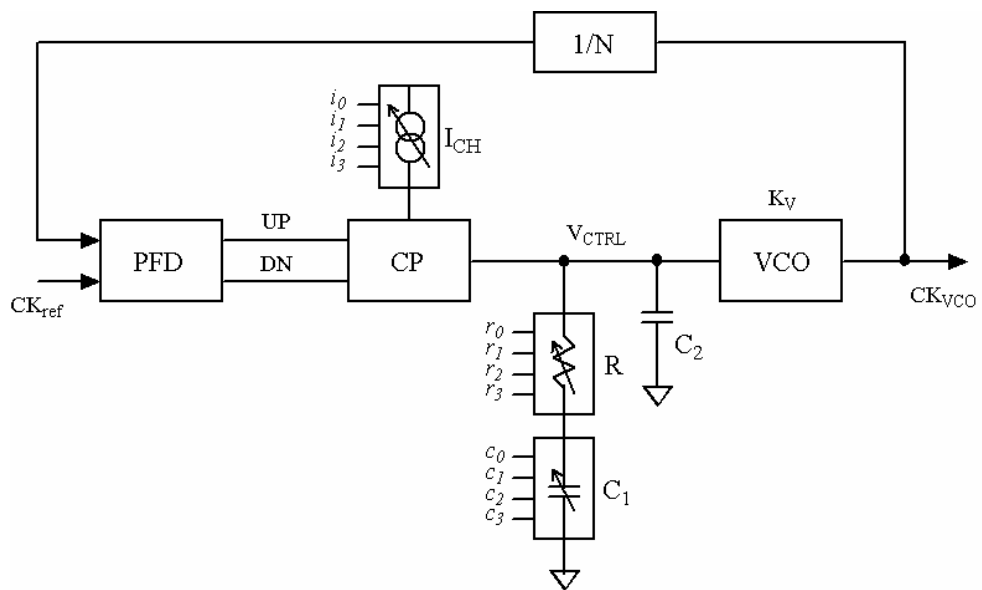


Figure 5.1: Adaptive bandwidth PLL block diagram.

R , and the capacitor C_1 . For every adjustable component, a 4-bit control signal results in sixteen different values of the adjustable parameter. Different combinations result in varied bandwidths and modified damping factor values. To abet high speed operations, the phase frequency detector (PFD), the charge pump (CP) and the frequency divider ($1/N$) are designed with special care and heightened attention.

Tuned oscillators in general are known to provide higher frequency stability and spectral purity at a given power level [47]. The negative resistance based CMOS LC oscillator is realized using a differential topology. Cross coupled PMOS and NMOS transistor pairs are used in parallel to achieve the negative resistance required to compensate for the losses in the tank circuit. NMOS and PMOS transistors are sized to achieve identical values of transconductance. The cross coupled configuration shown in Fig. 5.2, operates without a current source and was selected owing to its good phase noise performance and a large tuning range [48]. The VCO tuning characteristic is illustrated in Fig. 5.3. The VCO achieves a peak-to-peak output of 2.5 V and a tuning range of 2.85-3.19 GHz as the control voltage is swept from 1 to 2.5 V while demonstrating a gain (K_V) of 244 MHz/V.

Detailed design of an LC tank VCO in 0.5 μm n-well CMOS is presented in [49] that monolithically integrates the inductor. Figure 5.4 shows the microphotograph of the 1.8 GHz LC-VCO chip. The tuning characteristics are shown in Fig. 5.5 comparing both simulated and experimental behavior. Figure 5.6 shows the observed LC-VCO oscillations with a 1.757 GHz frequency on the digital oscilloscope. It is to be noted that design of 1.8 GHz in 0.5 μm n-well CMOS can be easily extended for designing 3 GHz LC-VCO in 0.25 μm n-well CMOS [50].

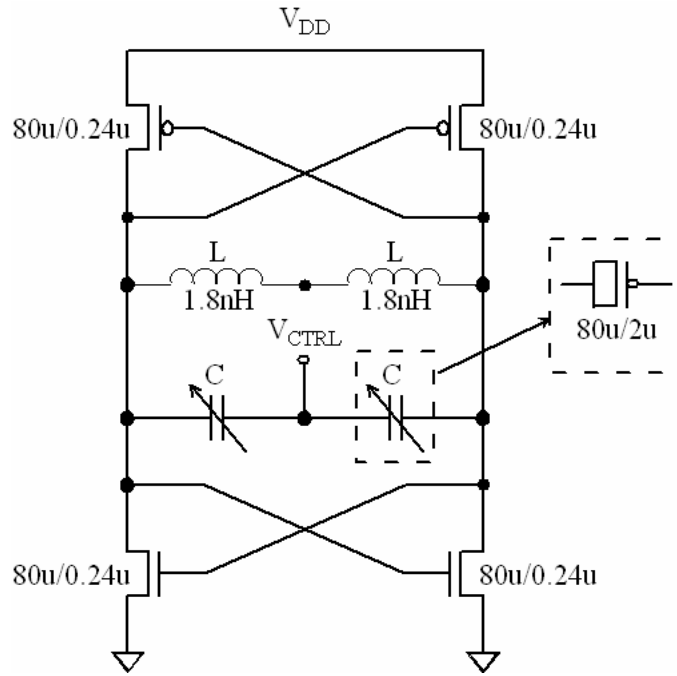


Figure 5.2: LC-VCO circuit with PMOS varactors.

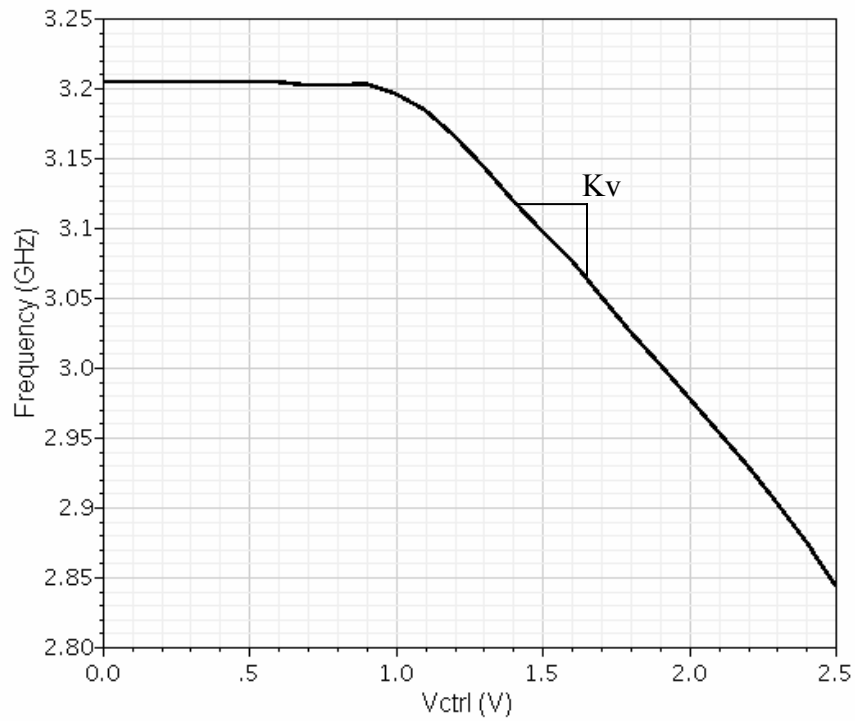


Figure 5.3: Simulation result of the LC-VCO tuning characteristic.

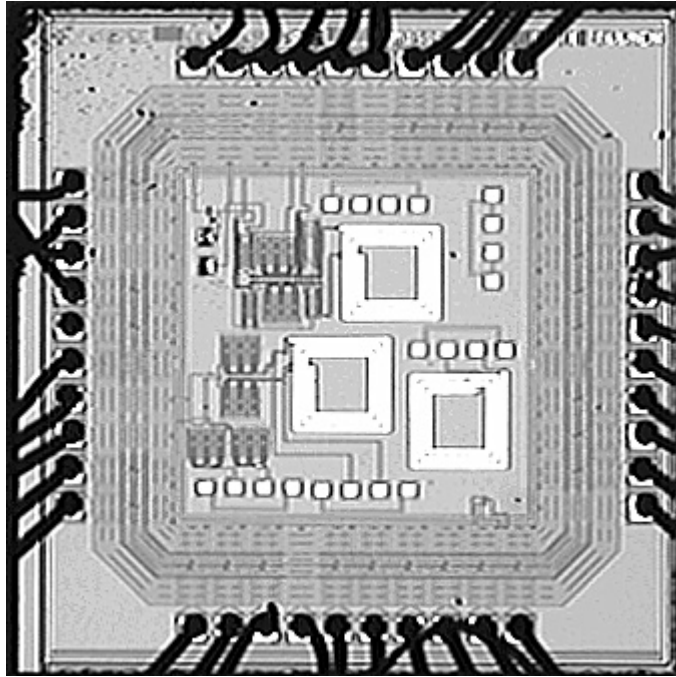


Figure 5.4: Microphotograph of the 1.8 GHz CMOS LC VCO chip.

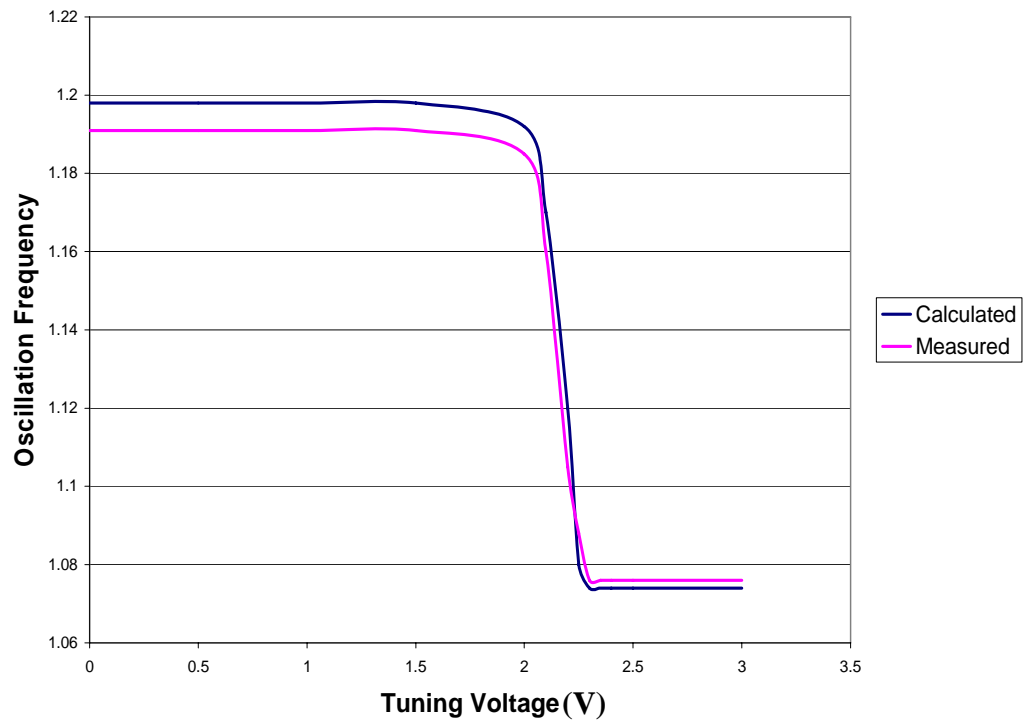


Figure 5.5: Simulation and measurement results of LC-VCO tuning characteristics.

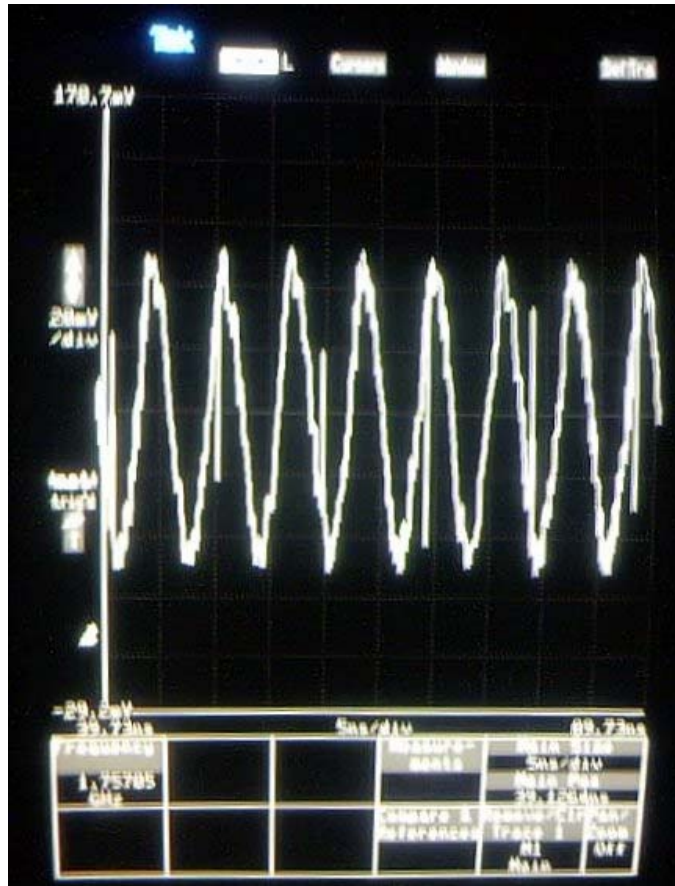


Figure 5.6: Oscillator output as observed on the digital sampling oscilloscope.

Conventional frequency dividers fail to operate accurately at high frequencies. In order to support an operating frequency of 3 GHz, a divide-by-64 dynamic divider with an inherent ability to operate at high frequencies was adapted [51, 52]. Figure 5.7 shows the divide-by-two cell of the divider. The divide-by-64 divider consists of six divide-by-two cells. The same structure can be used with a sinusoidal input clock without any modifications. The phase frequency detector is also modified for high speed operation which is shown in Fig. 5.8. A balanced (up/dn) switch structure and a unit gain stage are adopted in the charge pump block in order to further improve the charge pump performance. The circuit diagram of the charge pump and the unit gain cell are shown in Figs. 5.9 (a) and (b), respectively.

5.2 Simulated Phase Noise and Jitter Behavior of the Adaptive Bandwidth PLL

Phase noise and jitter performance of the proposed PLL is studied by adjusting its loop parameters. Such a study would then enable us to reduce the phase noise and timing jitter of a second order PLL by controlling its loop parameters. The relation between the output phase noise and loop bandwidth for offset frequencies of 1 MHz and 10 KHz is shown in Figs. 5.10 and 5.11, respectively. It can be observed that for an offset frequency of 1 MHz, the phase noise decreases as the loop bandwidth increases. For the two primary noise sources affecting the PLL performance, it can be deduced that at higher offset frequencies, the output noise is solely dominated by the VCO noise. A higher loop bandwidth is therefore desired to suppress the phase noise resulting from the VCO noise. A decrease in the output phase noise can also be observed with an increase in resistor, R and charge pump current, I_{CH} . Evidently, one can then exploit this phenomenon to design the PLL loop parameters for reduced output phase noise. On the other hand, for a lower offset frequency, e.g. 10 KHz, the phase noise approaches a constant value. This behavior at lower offset frequencies is primarily due to a dominance of the input reference clock noise. However, this component bears less relevance in the context of the PLL's loop

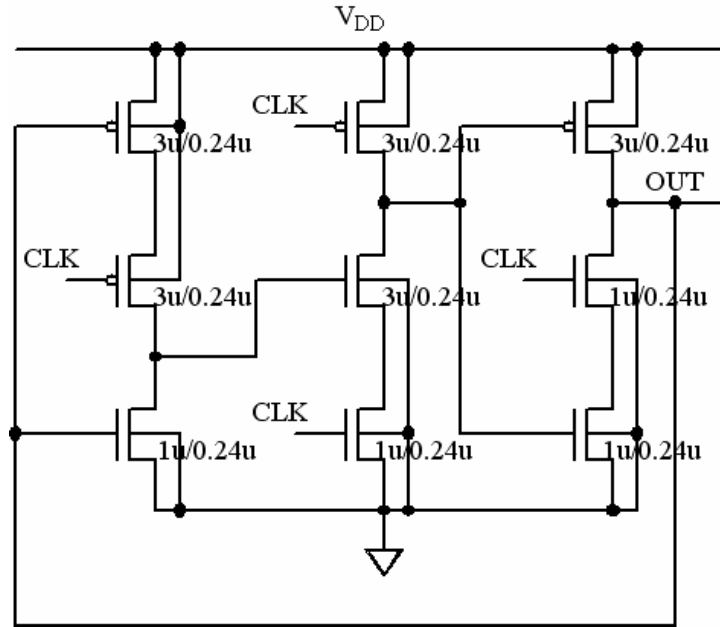


Figure 5.7: Divide-by-two cell of the dynamic divider.

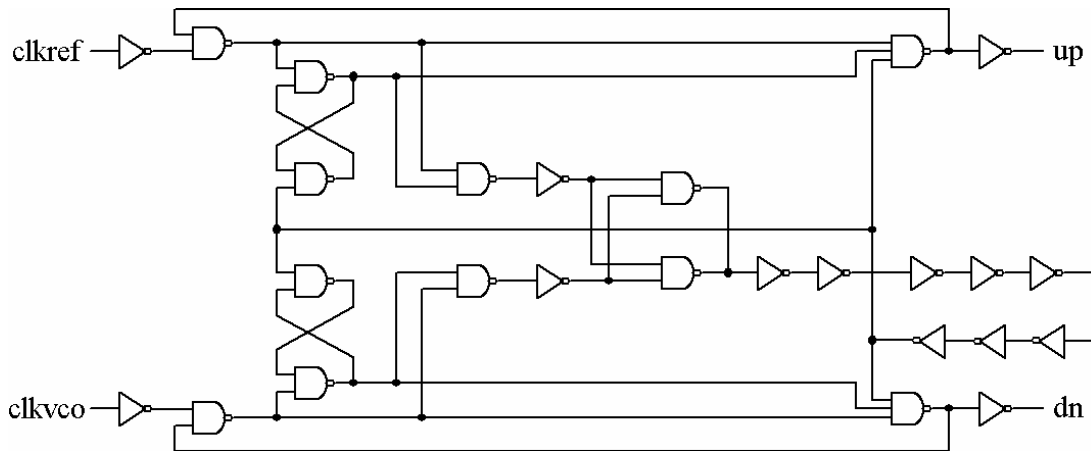
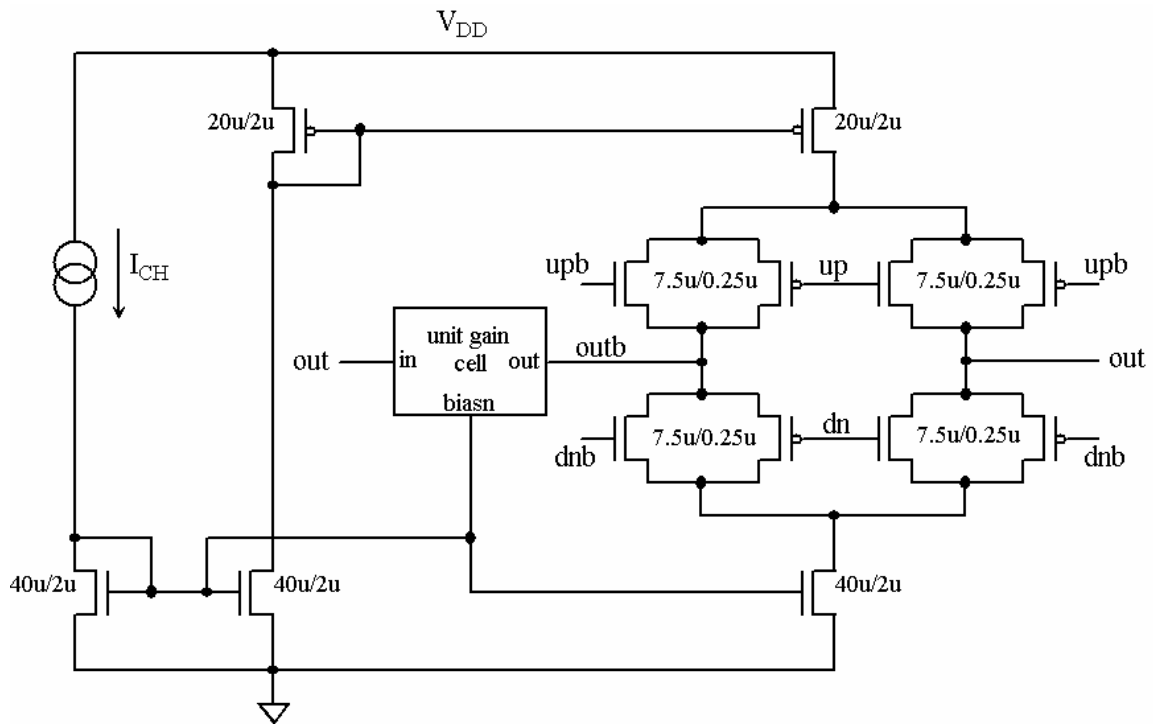
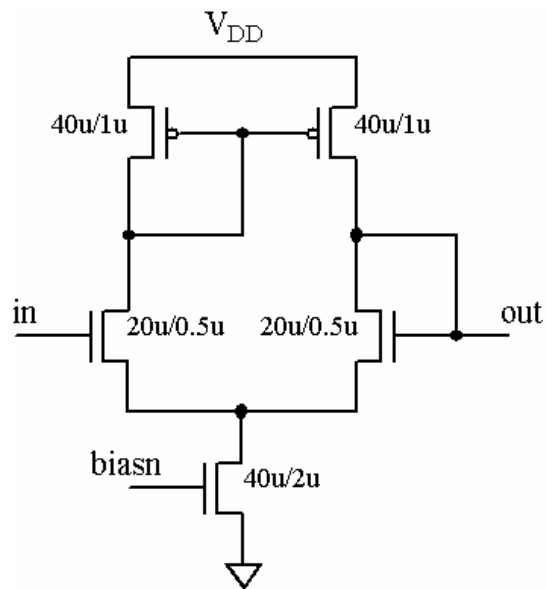


Figure 5.8: The logic level diagram of the phase frequency detector.



(a)



(b)

Figure 5.9: The circuit diagram of (a) the charge pump and (b) unit gain cell.

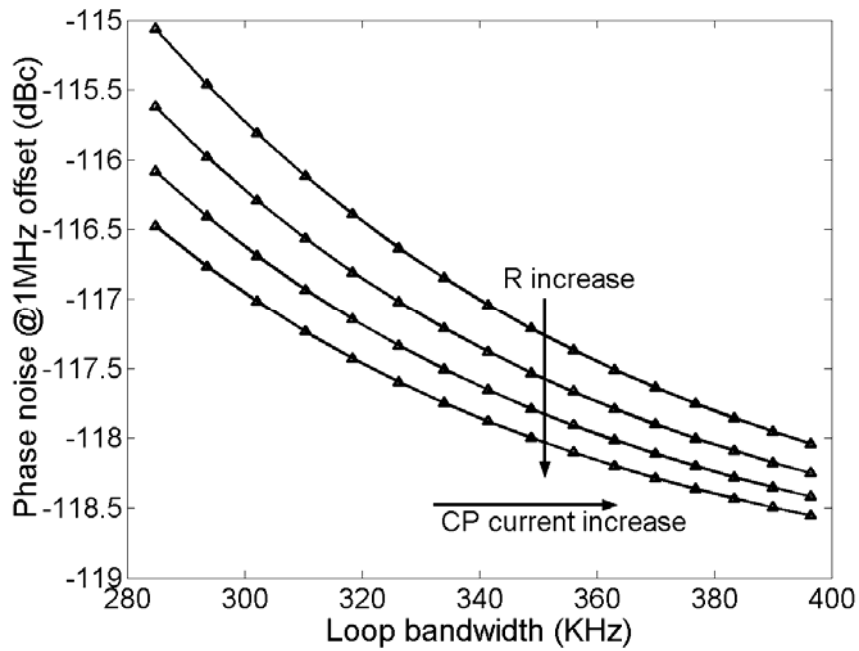


Figure 5.10: Relation between the output phase noise and the loop parameters at 1 MHz offset frequency.

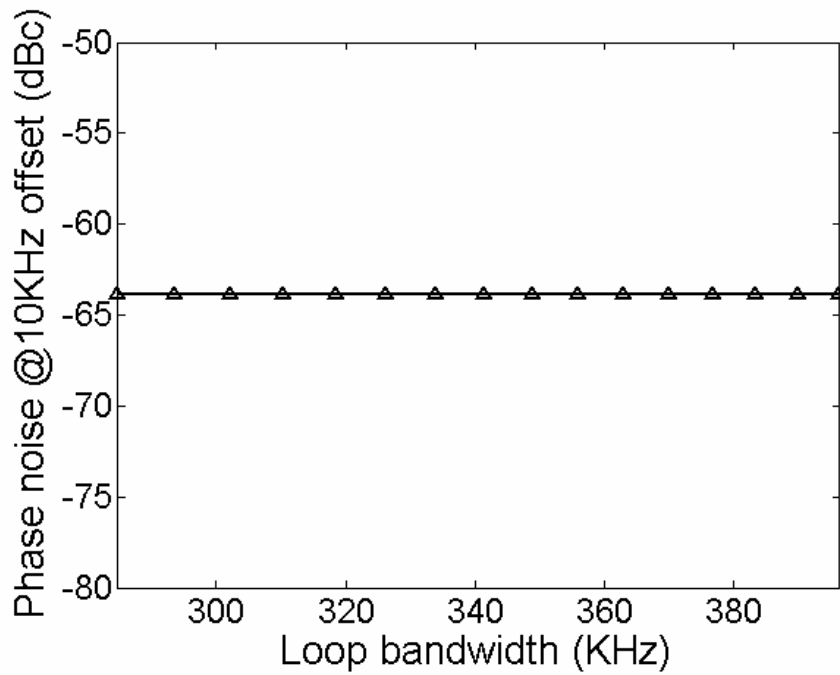


Figure 5.11: The relation between the output phase noise and the loop parameters at 10 KHz offset frequency.

parameters and is more related to the PLL noise by itself.

One can also note that a change in the capacitor, C_l causes little or no change in the phase noise performance. Also, from Eq. (3.3), it is imperative that, if a large loop bandwidth is desired to reduce the phase noise caused by noise in the VCO, it is more beneficial to increase the charge pump current I_{CH} rather than reducing the loop filter capacitance.

The behavior of long term RMS jitter due to VCO noise for various loop parameters is shown in Fig. 5.12. The product of the loop bandwidth and the damping factor $\omega_n \zeta$ is used to simplify the problem. This product is a function of charge pump current I_{CH} and the loop filter resistor R, but is not affected by the loop filter capacitance. The contour plot of the long term RMS jitter due to VCO noise for various I_{CH} and R values is shown in Fig. 5.13. The timing jitter decreases continuously for increasing values of I_{CH} and R.

This section addresses the effects of variations in the loop parameters on timing jitter and phase noise in a PLL. LC VCOs demonstrate good phase noise immunity at the cost of greater real estate and increased power consumption. Both jitter and phase noise exhibit a decrease with an increase in the charge pump current and the loop filter resistor. Though, the resulting increase in bandwidth corroborates the act of suppressing VCO noise it does little in reducing input reference clock noise.

Furthermore, increased values of I_{CH} and R command heightened levels of power consumption; a formidable challenge in the power versus performance paradigm. It can be further emphasized, that suitable values of the damping factor need to be selected to achieve faster locking, hence faster PLLs. An experimental study of the phase noise and timing jitter carried out by adjusting the loop parameters of the proposed PLL structure will then yield an optimum operating point for best noise performance.

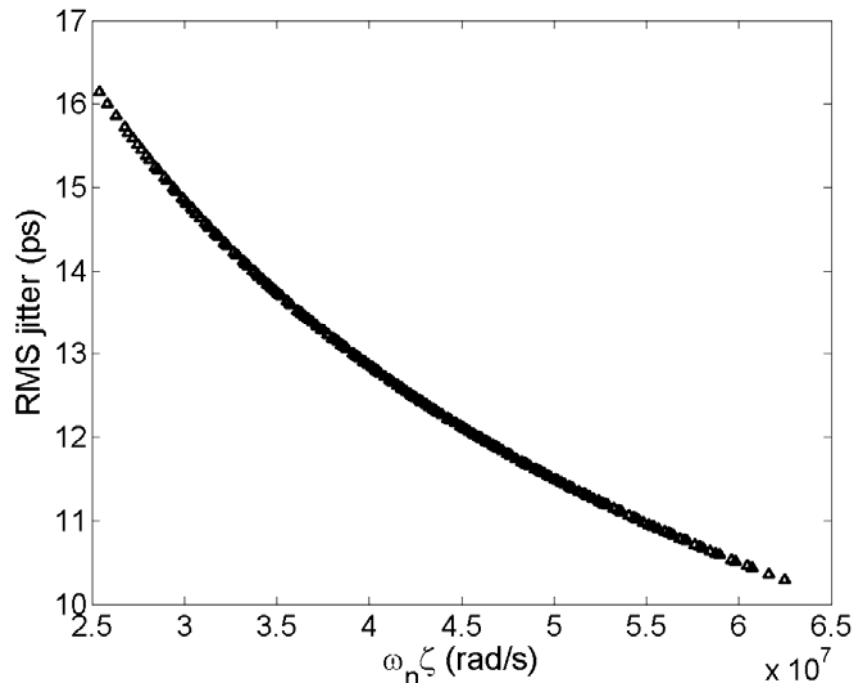


Figure 5.12: Variation of long term RMS jitter due to VCO noise for various loop bandwidth and damping factor products.

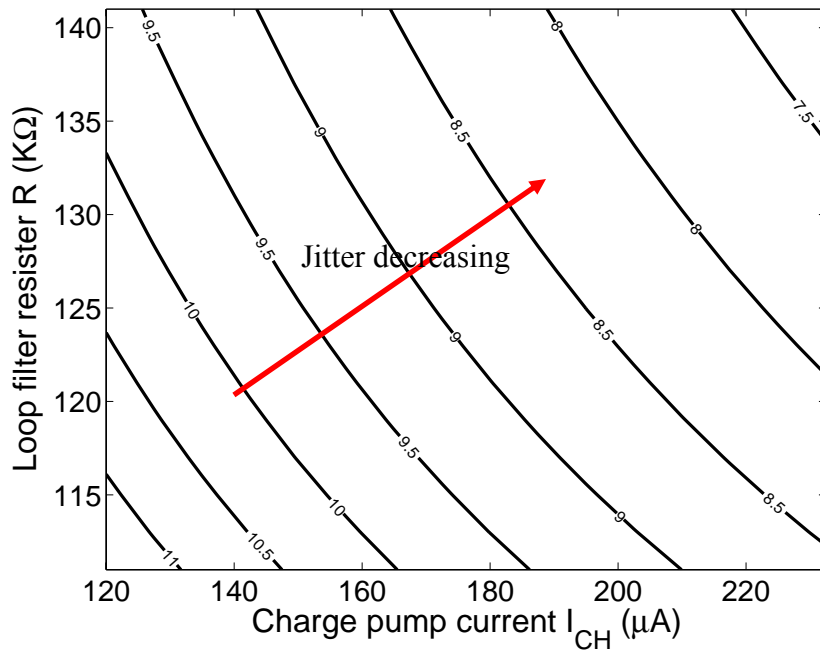


Figure 5.13: Contour plot of long term RMS jitter due to VCO noise for various charge pump current I_{CH} and loop filter resistance R .

5.3 Impact of Inductor Quality Factor on the Phase Noise Performance of PLL

For the LC tank VCO, the noise properties of the VCO itself can be modeled using the Leeson phase noise density expression [53]:

$$L(\Delta f) = \left(\frac{1}{8Q^2} \right) \left(\frac{FkT}{P} \right) \left(\frac{f_0}{\Delta f} \right)^2 \quad (5.1)$$

where F is the circuit noise factor, k is the Boltzman's constant, T is the temperature, P is the oscillator output power, Q is the quality factor of the LC tank, f_0 is the oscillation frequency, and Δf is the frequency offset from f_0 . It is evident from the above expression that performance enhancements and heightened frequency stability is a consequence of high Q -factor, increased output power and reduced circuit noise factor. This work chooses to focus on geometry based optimization schemes for inductor Q -factor enhancement. Such marked gains manifested in the quality factor performance result in a quadratic improvement in the phase noise performance. At large frequency offsets the VCO noise dominates the PLL phase noise. Hence an improvement in the Q -factor of the LC tank demonstrates an overall reduction of the PLL phase noise.

Simulation results of Q -factors are obtained for several inductors designed with outer diameters varying from 150 – 300 μm , line widths varying from 10 μm to 24 μm , inter-winding space of 1- 3 μm for an inductance value of 1.8 nH and the highest quality factor possible. The quality factor was studied as a function of the inductance and outer dimension to arrive at design guidelines for realizing close to optimum planar inductors. The resulting quality factor values are applied in context of the VCO and the overall PLL structure for studying their phase noise behavior.

A typical spiral inductor is illustrated in Fig. 5.14 with geometric parameters shown. Q -factor simulation results for different geometric parameters are shown in Fig. 5.15 with ascending Q -factors. Each index number on x-axis corresponds to a (d_{out} , W , S , N) combination,

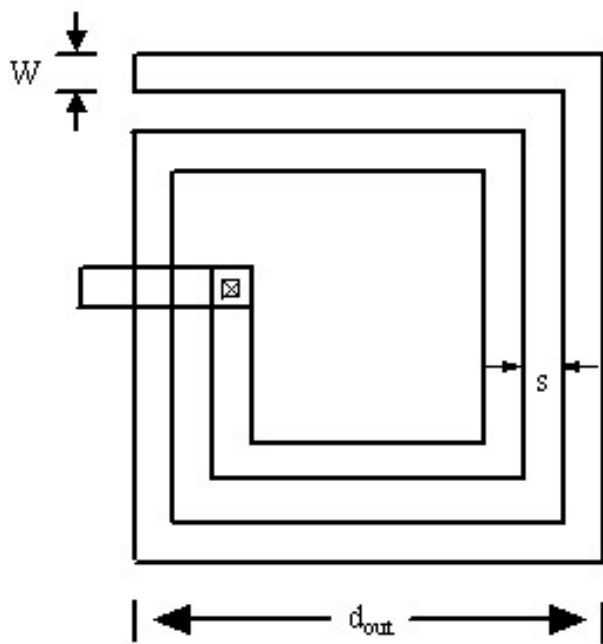
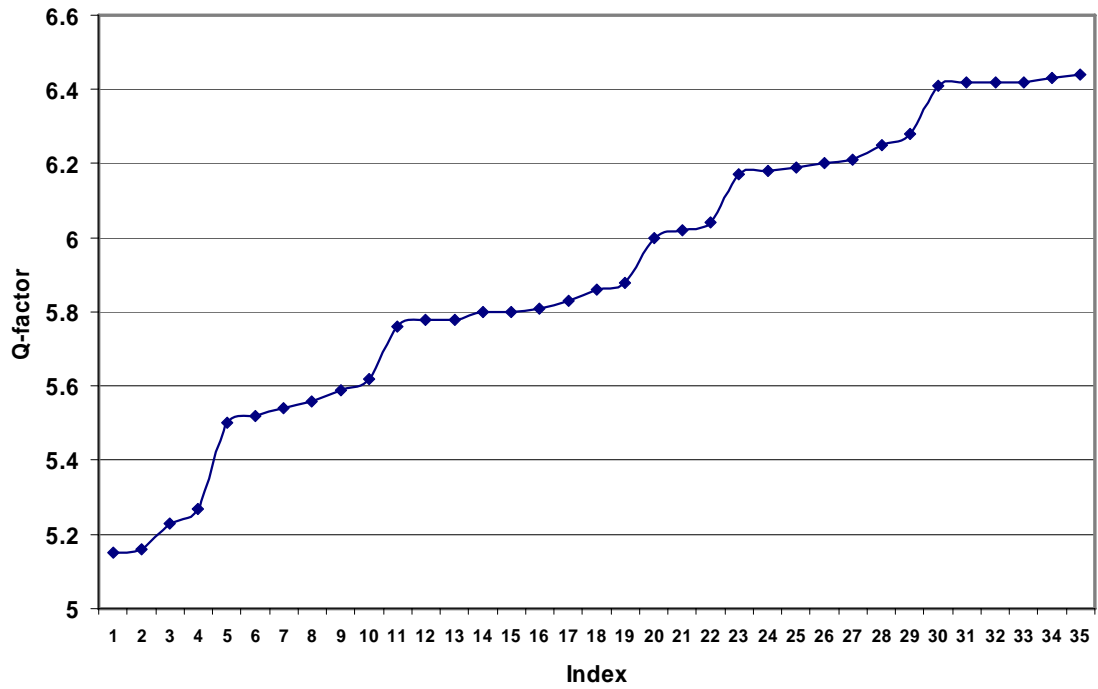


Figure 5.14: Square spiral with typical geometric parameters.



Index	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Length (um)	150	150	150	150	250	250	250	250	200	200	250	250	250	200	250	250	200	200
Width (um)	11	12	12	12	12	12	12	12	12	12	13	13	13	13	13	13	13	13
Spacing (um)	1.5	1.5	1	0.5	3	2.5	2	1.5	3	2.5	2.5	1.5	2	2.5	1	0.5	2	1.5
No. of Turns, N	3.25	3.5	3.5	3.25	1.75	1.75	1.75	1.75	2.25	2.25	1.75	1.75	1.75	2.25	1.75	1.75	2.25	2.25
Q	5.15	5.16	5.23	5.27	5.5	5.52	5.54	5.56	5.59	5.62	5.76	5.78	5.78	5.8	5.8	5.81	5.83	5.86

Index	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
Length (um)	200	250	200	200	300	300	300	300	200	200	200	300	300	300	300	300	300
Width (um)	13	14	14	14	14	14	14	14	15	15	15	15	15	15	15	15	15
Spacing (um)	1	0.5	1	0.5	3	2.5	2	1.5	3	2.5	2	3	0.5	1	2.5	2	1.5
No. of Turns, N	2.25	1.75	2.25	2.25	1.5	1.5	1.5	1.5	2.5	2.5	2.5	1.5	1.5	1.5	1.5	1.5	1.5
Q	5.88	6	6.02	6.04	6.17	6.18	6.19	6.2	6.21	6.25	6.28	6.41	6.42	6.42	6.42	6.43	6.44

Figure 5.15: Q-factor simulation results for different geometric parameters.

where d_{out} represents the length of outer diameter, W is the line widths, S is the inter-winding space and N represents the number of turns for the spiral inductor. Figure 5.16 shows the phase noise simulation results for the proposed PLL based on different Q-factors. An maximal Q-factor results in the optimal phase noise performance for the PLL.

5.4 Summary

This chapter addresses the effects of variations in the loop parameters on timing jitter and phase noise in a PLL. LC VCOs demonstrate good phase noise immunity at the cost of greater real estate and increased power consumption. Both jitter and phase noise exhibit a decrease with an increase in the charge pump current and the loop filter resistor. Though, the resulting increase in bandwidth corroborates the act of suppressing VCO noise it does little in reducing input reference clock noise. Furthermore, increased values of I_{CH} and R command heightened levels of power consumption; a formidable challenge in the power versus performance paradigm. It can be further emphasized, that suitable values of the damping factor need to be selected to achieve faster locking, hence faster PLLs. An experimental study of the phase noise and timing jitter carried out by adjusting the loop parameters of the proposed PLL structure will then yield an optimum operating point for best noise performance. Q-factor of the inductor in the VCO also affects the PLL phase noise performance. By carefully choosing the geometric parameters of the spiral inductor, and maximal Q-factor can be achieved which results in the optimal phase noise performance of the PLL.

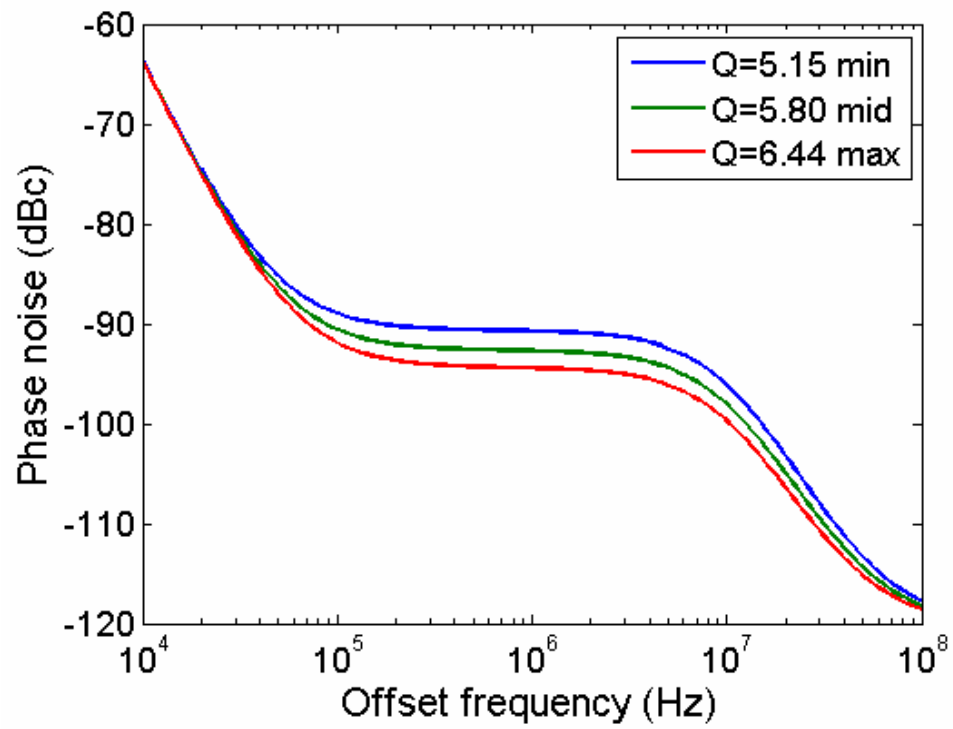


Figure 5.16: PLL phase noise simulation results for different Q-factors of the spiral inductor used in LC-VCO.

CHAPTER 6

SUMMARY AND SCOPE FOR FUTURE WORK

In this work, the noise and jitter issues in submicron CMOS phase-locked loop circuits have been studied from different aspects. A summary is given as follows.

6.1 Hot Carrier Effects on Phase Noise and Jitter in VCO

The degradation model of jitter and phase noise in CMOS ring oscillator based VCO due to hot carrier stress is developed. The VCO performance degradation includes decrease in the operation frequency, decrease in the tuning range and increase in jitter and phase noise. Simulation results show that there is a several dB increase in phase noise after hot carrier stress. The phase noise models developed in the present work is very useful in phase noise analysis for CMOS based OFDM systems based on hot carrier effects.

Furthermore, different CMOS VCOs with the oscillation mode and hot carrier stress mode are designed in 0.5 μm n-well CMOS process. The comparison of tuning characteristic and jitter performance before and after the hot carrier stress was performed. The experimental results verify the degradation in oscillation frequency and jitter performance of VCO. After four hours hot carrier stress, the oscillation frequency decreased by about 5 MHz and the RMS jitter increased by about 40 ps. Since VCO is an essential building block of PLL, the results of the work would be very useful in design of robust submicron CMOS PLL circuits.

6.2 Hot Carrier Effects on Phase Noise and Jitter in PLL

An attempt has been made to develop phase noise and jitter predication method for a second order PLL. Then hot carrier induced degradation on single-ended current starved VCO gain is studied. Analytical results of hot carrier induced effects on tracking performance, phase noise and jitter in PLL circuit designed in 0.25 μm N-well CMOS process are presented.

The analytical models which take into consideration hot carrier effects have shown that after a four hours stress, the gain of a current-starved VCO degrades from 1575 MHz/V to 940 MHz/V, which is about a 40% decrease in gain at an oscillation frequency of 800 MHz. In the following, the loop dynamics, phase noise and output clock jitter of a second order PLL are studied using s-domain analysis for a feedback control system. The degradation on PLL loop parameters and noise properties are analyzed for a second order PLL with a center frequency of 800 MHz, loop bandwidth of 16 MHz. The loop parameters, i.e., the loop bandwidth and damping factor decrease by about 23% after stress, which in turn decrease the loop bandwidth and increase the tracking time, respectively. The degradation causes a noticeable increase in phase noise at a lower offset frequency, 1 dB increase at 8 MHz offset, and a left-shifting peak of phase noise power spectral density.

Hot carrier induced degradation on VCO gain also influences the jitter properties of PLL. The most significant degradation occurs when the measurement interval is around 35 clock cycles, which gives about 17% increase in total output RMS jitter.

6.3 Experimental Study of Phase Noise in PLL

It is shown that the building blocks of a PLL contribute to its overall output noise which can be predicted by the graphical treatment of each noise source. The important noise sources are input reference clock, VCO and the frequency divider. Different PLLs with different VCOs have been designed fabricated in 0.5 μm CMOS technology. For the PLL with differential VCO, the measured output phase noise has a peak near the predicted loop bandwidth of 267 kHz. It follows the predicted noise behavior though the peak is narrower than the predicted curve. On the other hand, for the PLL with single-ended VCO which has larger bandwidth, there is no peak observed in phase noise curves. The measured phase noise data flatten out at the predicted peak position,

i.e. 462 kHz; however, the measured behavior follows the predicted PLL noise performance. The higher bandwidth of PLL with single-ended VCO suppresses the VCO noise.

The measurement result of PLL phase noise matches the predicted phase noise value. Therefore, the graphical treatment method is verified to be a useful tool to predict the PLL phase noise on the circuit design phase.

6.4 Phase Noise and Jitter Analysis of an Adaptive Bandwidth LC-VCO Based PLL

A 3 GHz adaptive bandwidth PLL with an LC-VCO is designed in a 0.25- μm *N*-well CMOS process. Adjustable charge pump and loop filter components are designed with the adaptive bandwidth feature in mind. Noise analysis on this PLL addresses the effects of variations in the loop parameters on timing jitter and phase noise in a PLL. LC VCOs demonstrate good phase noise immunity at the cost of greater real estate and increased power consumption. Both jitter and phase noise exhibit a decrease with an increase in the charge pump current and the loop filter resistor. Though, the resulting increase in bandwidth corroborates the act of suppressing VCO noise it does little in reducing input reference clock noise. Furthermore, increased values of I_{CH} and R command heightened levels of power consumption; a formidable challenge in the power versus performance paradigm. It can be further emphasized, that suitable values of the damping factor need to be selected to achieve faster locking, hence faster PLLs.

An experimental study of the phase noise and timing jitter is carried out by adjusting the loop parameters of the proposed PLL structure which will then yield an optimum operating point for best noise performance.

Moreover the quality factor Q of the inductor in the LC VCO is an important factor for the VCO phase noise performance. Geometric parameters of on-chip spiral inductor affect the Q -factor. Simulation results show that a higher Q -factor is desired for better PLL phase noise performance.

6.5 Scope for the Future Work

Noise analysis on hot carrier effects can be extended to higher order PLL and PLL with LC-VCO structure. Hot-hole analysis and the negative bias temperature instability (NBTI) in P-MOSFETs can also be applied to complete this noise study on small dimension devices. Low voltage CMOS design strategies can be applied to reduce the stress voltage on drain and gate of MOSFETs, which may reduce the generation of hot carriers. Therefore, the hot carrier induced device degradation can be minimized. For short channel MOS devices, there are other effects besides the hot carrier effect which may also affect the VCO and PLL performance. For example, the radiation effect and the temperature dependence on device parameters are also reasons that cause device degradation. Studies on these effects may also be very useful in submicron/deep submicron PLL circuit design.

The phase noise prediction method can be more accurate if all the noise sources in PLL are considered including phase frequency detector noise and charge pump noise. Moreover, the noise analysis on a higher order (third order) PLL model will further improve the accuracy of prediction. In this work, phase noise and jitter of PLL system are modeled by a linear noise model. Nonlinear noise model for PLL phase noise and jitter analysis should be developed in future work for improved PLL design. Experimental study on the adaptive bandwidth PLL can be useful in PLL design achieving phase noise and jitter optimization and is suggested for the future work. The phase noise and jitter model developed can be also used in communication system noise analysis.

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APPENDIX A

MOSIS SPICE MOS MODEL PARAMETERS FOR STANDARD N-WELL CMOS TECHNOLOGY

The following SPICE MOS Model parameters used in simulation have been obtained from the website: www.mosis.org. Both 0.5 μm and 0.25 μm N-well CMOS process parameters are used in SPICE simulations.

RUN: T66H

TECHNOLOGY: SCN05

VENDOR: AMIS

FEATURE SIZE: 0.5 microns

```
.MODEL CMOSN NMOS (
+VERSION = 3.1          TNOM = 27          LEVEL = 8
+XJ = 1.5E-7           NCH = 1.7E17       TOX = 1.42E-8
+K1 = 0.8738536       K2 = -0.0897544       VTH0 = 0.6560917
+K3B = -8.2202383    W0 = 1.07093E-8      K3 = 21.9401867
+DVT0W = 0           DVT1W = 0           NLX = 1E-9
+DVT0 = 2.7227001    DVT1 = 0.4670998    DVT2W = 0
+U0 = 461.6553119    UA = 1E-13          DVT2 = -0.1723153
+UC = 6.856484E-12   VSAT = 1.754942E5    UB = 1.885415E-18
+AGS = 0.1342215     B0 = 2.432492E-6     A0 = 0.6562813
+KETA = -4.895559E-3 A1 = 1.408389E-6     B1 = 5E-6
+RDSW = 1.416242E3   PRWG = 0.0258829    A2 = 0.3288324
+WR = 1              WINT = 2.303158E-7   PRWB = 9.26143E-3
+XL = 1E-7           XW = 0              LINT = 7.539811E-8
+DWB = 2.445322E-8   VOFF = -0.0249483   DWG = -9.083581E-9
+CIT = 0             CDSC = 2.4E-4        NFACTOR = 0.8038617
+CDSCB = 0           ETA0 = 1.964245E-3   CDSCD = 0
+DSUB = 0.0658933   PCLM = 2.6210459    ETAB = -2.023215E-4
+PDIBLC2 = 2.645412E-3 PDIBLCB = -1.346078E-4 PDIBLC1 = 0.7368181
+PSCBE1 = 6.61584E8  PSCBE2 = 2.949145E-4 DROUT = 0.9458376
+DELTA = 0.01       RSH = 81.5          PVAG = 0
+PRT = 0            UTE = -1.5          MOBMOD = 1
+KT1L = 0           KT2 = 0.022         KT1 = -0.11
+UB1 = -7.61E-18    UC1 = -5.6E-11      UA1 = 4.31E-9
+WL = 0             WLN = 1             AT = 3.3E4
+WWN = 1           WWL = 0             WW = 0
+LLN = 1           LW = 0              LL = 0
+LWL = 0           CAPMOD = 2          LWN = 1
+CGDO = 2.09E-10    CGSO = 2.09E-10     XPART = 0.5
+CJ = 4.284376E-4   PB = 0.9184348      CGBO = 1E-9
+CJSW = 3.091424E-10 PBSW = 0.8           MJ = 0.4389925
+CJSWG = 1.64E-10  PBSWG = 0.8         MJSW = 0.2075303
                   MJSWG = 0.2075303
```

+CF = 0 PVTH0 = 0.0584953 PRDSW = 105.8848326
+PK2 = -0.0258839 WKETA = -0.0190782 LKETA = 3.015064E-3)

.MODEL CMOS PMOS (LEVEL = 8
+VERSION = 3.1 TNOM = 27 TOX = 1.42E-8
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9528605
+K1 = 0.5317022 K2 = 0.0124917 K3 = 6.3482082
+K3B = -0.6416794 W0 = 1.284945E-8 NLX = 2.886738E-8
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.9392328 DVT1 = 0.4759313 DVT2 = -0.1149682
+U0 = 228.5251718 UA = 3.371715E-9 UB = 1.163631E-21
+UC = -5.4908E-11 VSAT = 1.511601E5 A0 = 0.885904
+AGS = 0.1525682 B0 = 1.020429E-6 B1 = 5E-6
+KETA = -1.92493E-3 A1 = 3.694952E-4 A2 = 0.3198543
+RDSW = 3E3 PRWG = -0.0411377 PRWB = -0.02081
+WR = 1 WINT = 2.951834E-7 LINT = 1.038473E-7
+XL = 1E-7 XW = 0 DWG = -2.531739E-8
+DWB = 1.921818E-8 VOFF = -0.0776546 NFACTOR = 0.8439721
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.5617555 ETAB = -0.0589814
+DSUB = 1 PCLM = 2.0722197 PDIBLC1 = 0.0237211
+PDIBLC2 = 3.093135E-3 PDIBLCB = -0.0547993 DROUT = 0.1579219
+PSCBE1 = 5.292003E9 PSCBE2 = 5E-10 PVAG = 8.717958E-3
+DELTA = 0.01 RSH = 110.7 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.74E-10 CGSO = 2.74E-10 CGBO = 1E-9
+CJ = 7.259994E-4 PB = 0.9644989 MJ = 0.4989143
+CJSW = 2.585738E-10 PBSW = 0.99 MJSW = 0.3873857
+CJSWG = 6.4E-11 PBSWG = 0.99 MJSWG = 0.3873857
+CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424
+PK2 = 3.73981E-3 WKETA = 5.433522E-3 LKETA = -2.371979E-3)

RUN: T65V (MM_NON-EPI_THK-MTL)
TECHNOLOGY: SCN025

VENDOR: TSMC
FEATURE SIZE: 0.25 microns

.MODEL CMOS NMOS (LEVEL = 8
+VERSION = 3.1 TNOM = 27 TOX = 5.7E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3790539
+K1 = 0.4678673 K2 = 2.094882E-3 K3 = 1E-3
+K3B = 2.8635543 W0 = 1E-7 NLX = 1.952698E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.4891847	DVT1 = 0.5915719	DVT2 = -0.5
+U0 = 305.4959128	UA = -1.245181E-9	UB = 2.524523E-18
+UC = 4.296097E-11	VSAT = 1.326081E5	A0 = 1.6595933
+AGS = 0.3280687	B0 = -1.620759E-8	B1 = -1E-7
+KETA = -1.129018E-3	A1 = 1.358712E-4	A2 = 0.5058927
+RDSW = 200	PRWG = 0.3631279	PRWB = -0.0636973
+WR = 1	WINT = 0	LINT = 0
+XL = 0	XW = -4E-8	DWG = -2.075568E-8
+DWB = 2.088413E-9	VOFF = -0.0992525	NFACTOR = 1.3986948
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 6.307375E-3	ETAB = 2.812558E-4
+DSUB = 0.0453069	PCLM = 1.585851	PDIBLC1 = 0.9927926
+PDIBLC2 = 2.413581E-3	PDIBLCB = -0.0251233	DROUT = 0.9993683
+PSCBE1 = 8E10	PSCBE2 = 5.882417E-10	PVAG = 1.009375E-7
+DELTA = 0.01	RSH = 3.9	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 4.16E-10	CGSO = 4.16E-10	CGBO = 7E-10
+CJ = 1.740557E-3	PB = 0.99	MJ = 0.4621235
+CJSW = 4.180326E-10	PBSW = 0.8994981	MJSW = 0.2677227
+CJSWG = 3.29E-10	PBSWG = 0.8994981	MJSWG = 0.2677227
+CF = 0	PVTH0 = -8.458495E-3	PRDSW = -10
+PK2 = 4.057598E-3	WKETA = 5.254243E-5	LKETA = -8.084685E-3)

.MODEL CMOS PMOS (

+VERSION = 3.1	TNOM = 27	LEVEL = 8
+XJ = 1E-7	NCH = 4.1589E17	TOX = 5.7E-9
+K1 = 0.615586	K2 = 1.740055E-3	VTH0 = -0.5224091
+K3B = 10.126439	W0 = 1E-6	K3 = 0
+DVT0W = 0	DVT1W = 0	NLX = 7.427938E-9
+DVT0 = 2.6099192	DVT1 = 0.7749922	DVT2W = 0
+U0 = 100	UA = 9.628749E-10	DVT2 = -0.1505238
+UC = -1E-10	VSAT = 1.832587E5	UB = 1E-21
+AGS = 0.1473504	B0 = 4.332305E-7	A0 = 1.0636713
+KETA = 8.213399E-3	A1 = 0.0251405	B1 = 2.456784E-6
+RDSW = 1.048851E3	PRWG = 0.206411	A2 = 0.3
+WR = 1	WINT = 0	PRWB = -0.1916693
+XL = 0	XW = -4E-8	LINT = 2.731764E-8
+DWB = 6.772034E-11	VOFF = -0.118657	DWG = -4.035405E-8
+CIT = 0	CDSC = 2.4E-4	NFACTOR = 1.0750885
+CDSCB = 0	ETA0 = 0.2473215	CDSCD = 0
+DSUB = 1.0277572	PCLM = 1.2659136	ETAB = -0.0574668
		PDIBLC1 = 7.65712E-3

+PDIBLC2 = -1E-5	PDIBLCB = -1E-3	DROUT = 0.1043079
+PSCBE1 = 6.942941E10	PSCBE2 = 5E-10	PVAG = 2.330338E-3
+DELTA = 0.01	RSH = 3	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 4.99E-10	CGSO = 4.99E-10	CGBO = 7E-10
+CJ = 1.840957E-3	PB = 0.9809513	MJ = 0.4692719
+CJSW = 3.603168E-10	PBSW = 0.99	MJSW = 0.3266334
+CJSWG = 2.5E-10	PBSWG = 0.99	MJSWG = 0.3266334
+CF = 0	PVTH0 = 5.46428E-3	PRDSW = 1.8819543
+PK2 = 3.138577E-3	WKETA = 0.0321052	LKETA = -6.626532E-3)

APPENDIX B

DERIVATIONS OF JITTER AND PHASE NOISE MODEL IN RING OSCILLATORS AND PLL PHASE NOISE PREDICTION

Jitter and phase noise model for ring oscillators based on impulse sensitivity function (ISF) [15] has been used in Chapter 2 to study the hot carrier induced VCO degradation. Moreover, the phase noise and jitter prediction method [18] for PLL is discussed in Chapter 3. The derivations of the models are shown as follows.

B.1 Impulse Sensitivity Function (ISF)

The output of a practical oscillator can be written as

$$V_{out}(t) = A(t)f[\omega_0 t + \phi(t)] \quad (\text{B.1})$$

where the function f is periodic in 2π and $\phi(t)$. $A(t)$ models fluctuations in phase and amplitude due to internal and external noise sources. Consider the single-ended ring oscillator with a single current source on one of the node as shown in Fig. B.1.

Suppose that the current source consists of an impulse of current with area Δq (in coulombs) occurring at time $t = t_0$. This causes an instantaneous change in the voltage of this node, given by

$$\Delta V = \frac{\Delta q}{C_{node}} \quad (\text{B.2})$$

where C_{node} is the effective capacitance on that node. This produces a shift in phase. For small ΔV , the change in the phase $\phi(t)$ is proportional to the injected charge given by

$$\Delta \phi = \Gamma(\omega_0 t) \frac{\Delta V}{V_{swing}} = \Gamma(\omega_0 t) \frac{\Delta q}{q_{max}} \quad (\text{B.3})$$

where V_{swing} is the voltage swing across the node and $q_{max} = C_{node} V_{swing}$.

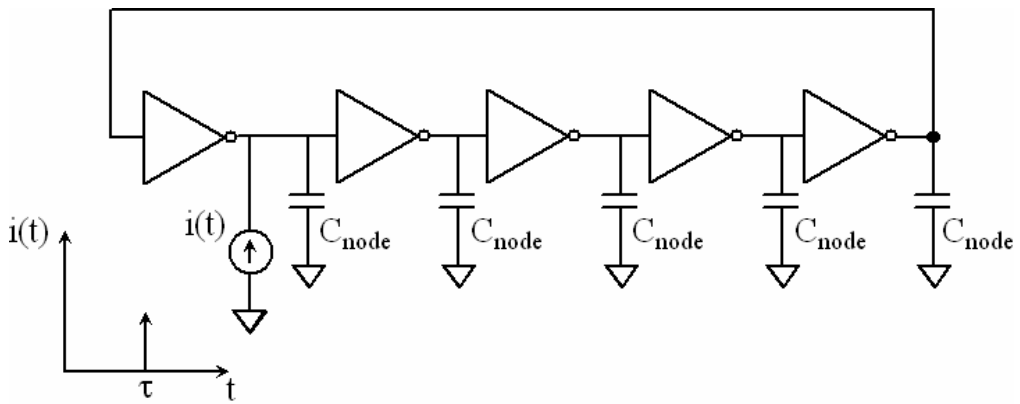


Figure B.1: Five-stage single-ended ring oscillator with current impulse injection.

The dimensionless function $\Gamma(\omega_0 t)$ is the time-varying proportionality constant and is called the impulse sensitivity function (ISF). Based on experimental study on ISF for ring oscillators in [15], the ISF can be approximated as triangular in shape and with symmetric rising and falling edges, as shown in Fig. B.2. The waveform $f(x)$ is the normalized periodic function in Eq. (B.1). The ISF has a maximum of $1/f'_{\max}$, where $1/f'_{\max}$ is the maximum slope of $f(x)$. Also, the width of the triangles is approximately $2/f'_{\max}$, and hence the slopes of the sides of the triangles are ± 1 . The relationship between $f(x)$ and $\Gamma(x)$ reveals the property that the maximum phase shift occurs when the impulse is injected during transition, and zero phase shift produced by an impulse injected at the peak, which has also been discussed in Chapter 2. Therefore, the averaged ISF, Γ_{rms} can be estimated as

$$\Gamma_{rms}^2 = \frac{1}{2\pi} \int_0^{2\pi} \Gamma^2(x) dx = \frac{4}{2\pi} \int_0^{1/f'} x^2 dx = \frac{2}{3\pi} \left(\frac{1}{f'_{\max}} \right)^3 \quad (\text{B.4})$$

On the other hand, stage delay is proportional to the rise time

$$t_D = \frac{\eta}{f'_{\max}} \quad (\text{B.5})$$

where t_D is the normalized stage delay and η is a proportionality constant. Consider a N stage ring oscillator, the total normalized delay is 2π . Therefore,

$$2\pi = 2Nt_D = \frac{2N\eta}{f'_{\max}} \quad (\text{B.6})$$

From Eqs. (B.4) and (B.6), the following approximate expression for Γ_{rms} is obtained:

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}} \frac{1}{N^{1.5}} \quad (\text{B.7})$$

The proportionality constant η is taken to be 0.75 in this work [14].

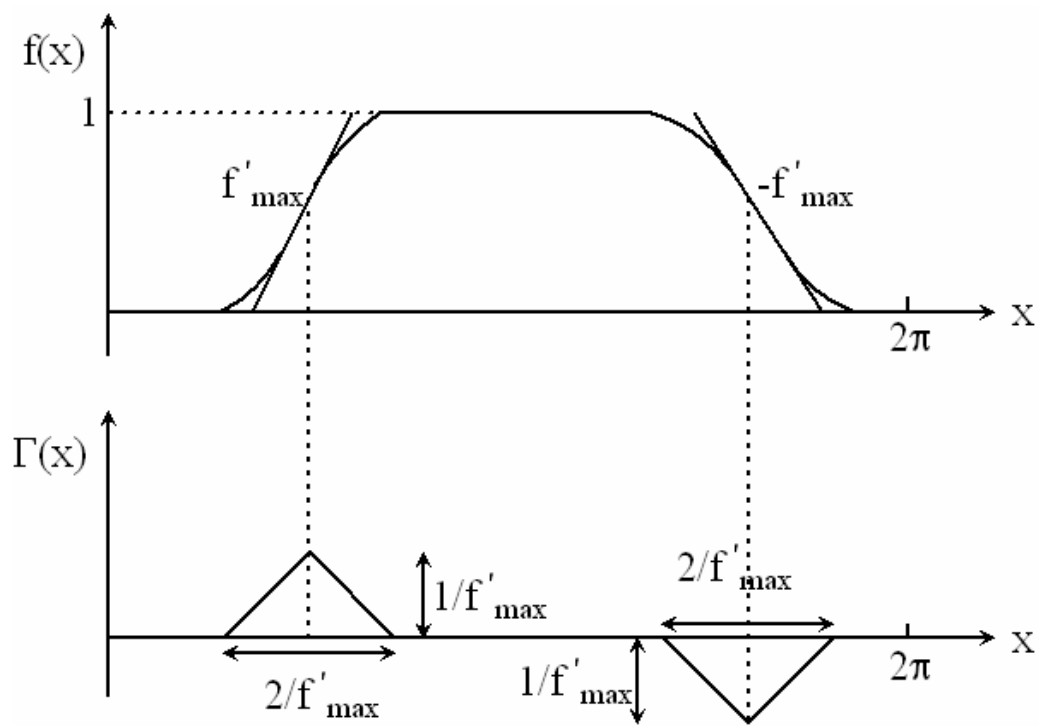


Figure B.2: Approximate waveform and ISF for ring oscillator.

B.2 Phase Noise Model for Ring Oscillator Based on ISF

The unit impulse response of the system is defined as the amount of phase shift per unit current impulse [14]. Based on the foregoing argument, we obtain the following time dependent impulse response for system shown in Fig. B.1:

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t - \tau) \quad (\text{B.8})$$

where $u(t - \tau)$ is a unit step. Knowing the response to an impulse, $\phi(t)$ can be calculated in response to any injected current using superposition integral

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau) i(\tau) d\tau = \int_{-\infty}^t \frac{\Gamma(\omega_0 \tau)}{q_{\max}} i(\tau) d\tau \quad (\text{B.9})$$

where $i(t)$ represents the noise current injected into the node of interest. Since the ISF is periodic, it can be expanded in a Fourier series

$$\Gamma(\omega_0 t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \quad (\text{B.10})$$

where the coefficients c_n are real-valued coefficients, and θ_n is the phase of the n^{th} harmonic, which is not important for random input noise and is thus neglected. From Eqs. (B.9) and (B.10), we obtain

$$\phi(t) = \frac{1}{q_{\max}} \left[\frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 \tau) d\tau \right] \quad (\text{B.11})$$

Now suppose that a sinusoidal perturbation current $i(t)$ is injected into the node of interest at a frequency of $n\omega_0 + \Delta\omega$. We have $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$, where n can change from 0 to ∞ . Suppose ω_0 is relatively high, therefore $\phi(t)$ is given by

$$\begin{aligned}
\phi(t) &= \frac{1}{q_{\max}} \left[\frac{c_0}{2} \int_{-\infty}^t I_n \cos[(n\omega_0 + \Delta\omega)\tau] d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t I_n \cos[(n\omega_0 + \Delta\omega)\tau] \cos(n\omega_0\tau) d\tau \right] \\
&= \frac{1}{q_{\max}} \left[\frac{c_0 I_n \sin[(n\omega_0 + \Delta\omega)t]}{2(n\omega_0 + \Delta\omega)} + \sum_{n=1}^{\infty} \frac{c_n I_n}{2} \int_{-\infty}^t \{\cos[(2n\omega_0 + \Delta\omega)\tau] + \cos(\Delta\omega\tau)\} d\tau \right] \\
&= \frac{1}{q_{\max}} \left[\frac{c_0 I_n \sin[(n\omega_0 + \Delta\omega)t]}{2(n\omega_0 + \Delta\omega)} + \sum_{n=1}^{\infty} \frac{c_n I_n \sin[(n\omega_0 + \Delta\omega)t]}{2(n\omega_0 + \Delta\omega)} + \frac{c_n I_n \sin(\Delta\omega t)}{2\Delta\omega} \right] \\
&\approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{\max} \Delta\omega}
\end{aligned} \tag{B.12}$$

Therefore, an injected current at $n\omega_0 + \Delta\omega$ results in a pair of equal sidebands at $\omega_0 \pm \Delta\omega$ with a sideband power relative to the carrier given by

$$L(\Delta\omega) = 10 \log \left(\frac{I_n^2 c_n^2}{8q_{\max}^2 \Delta\omega^2} \right) \tag{B.13}$$

To carry out a quantitative analysis of the phase noise sideband power, now consider an input noise current with a white power spectral density $\overline{i_n^2} / \Delta f$. Note that I_n in (B.13) represents the peak amplitude, hence, $I_n^2 / 2 = \overline{i_n^2} / \Delta f$ for $\Delta f = 1\text{Hz}$. Based on Eq. (B.13), the total single sideband phase noise spectral density in dB below the carrier per unit bandwidth due to the source on one node at an offset frequency of $\Delta\omega$ is given by

$$L(\Delta\omega) = 10 \log \left(\frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{4q_{\max}^2 \Delta\omega^2} \right) \tag{B.14}$$

Now, according to Parseval's relation we have

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{B.15}$$

As a result

$$L(\Delta\omega) = 10 \log \left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2} / \Delta f}{2\Delta\omega^2} \right) \quad (\text{B.16})$$

This equation represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region of the phase noise spectrum. From Eqs. (B.7) and (B.16), and knowing the current noise spectrum, $\overline{i_n^2} / \Delta f$, the output phase noise of a ring oscillator can be calculated.

B.3 Jitter Model for Ring Oscillator Based on ISF

Normally, the standard deviation of the jitter after ΔT seconds is given as

$$\sigma_{\Delta T} = \kappa \sqrt{\Delta T} \quad (\text{B.17})$$

where κ is a proportionality constant determined by circuit parameters. In many applications, phase jitter, which is defined as

$$\sigma_{\Delta\phi} = \frac{2\pi}{T} \sigma_{\Delta T} = \omega_0 \sigma_{\Delta T} \quad (\text{B.18})$$

is a more useful measure. The calculation of phase jitter can be given as follows based on Eq. (B.9). Note,

$$\Delta\phi = \int_0^{\Delta T} \frac{\Gamma(\omega_0\tau)}{q_{max}} i(\tau) d\tau \quad (\text{B.19})$$

Then we have

$$\begin{aligned} \sigma_{\Delta\phi}^2 &= E\{\Delta\phi^2\} = E\{\phi(t + \Delta T) - \phi(t)\}^2 \\ &= \frac{1}{q_{max}^2} \int_0^{\Delta T} \int_0^{\Delta T} \Gamma(\omega_0\tau_1) \Gamma(\omega_0\tau_2) \cdot E[i(\tau_1)i(\tau_2)] d\tau_1 d\tau_2 \end{aligned} \quad (\text{B.20})$$

Note that for a white noise current source, the auto-correlation function is

$$R(t_1, t_2) = (1/2) (\overline{i_n^2} / \Delta f) \delta(t_1 - t_2), \text{ therefore,}$$

$$\sigma_{\Delta\phi}^2 = \frac{\overline{i_n^2} / \Delta f}{2q_{max}^2} \int_0^{\Delta T} \Gamma^2(\omega_0\tau) d\tau = \frac{\overline{i_n^2} / \Delta f}{2q_{max}^2} \cdot \Gamma_{rms}^2 \Delta T \quad (\text{B.21})$$

Now we have

$$\sigma_{\Delta T} = \frac{1}{\omega_0} \sigma_{\Delta\phi} = \frac{\Gamma_{rms}}{q_{max} \omega_0} \sqrt{\frac{1}{2} \cdot \frac{\overline{i_n^2}}{\Delta f}} \cdot \sqrt{\Delta T} \quad (\text{B.22})$$

$$\kappa = \frac{\Gamma_{rms}}{q_{max} \omega_0} \sqrt{\frac{1}{2} \cdot \frac{\overline{i_n^2}}{\Delta f}} \quad (\text{B.23})$$

From Eqs. (B.7) and (B.23), and knowing the current noise spectrum, $\overline{i_n^2} / \Delta f$, the output rms jitter of a ring oscillator can be calculated.

B.4 Phase Noise Prediction for PLL

There are two dominant sources of the noise which affect the phase noise of the output, VCO phase noise and the input reference phase noise. Assuming that the VCO phase noise is not correlated with the phase noise of the input, the phase noise power spectrum at the output can be calculated using superposition. The output phase noise due to each source can be evaluated independently and the total phase noise is the sum of them. This method of PLL phase noise prediction is also called the graphical treatment.

Assuming a noiseless input and a noisy VCO dominated by its $1/f^2$ noise, the equivalent phase domain model of PLL is shown in Fig. B.3. In the equivalent noise model of a VCO, $n_0(s)$ is the input noise source. The effect of VCO phase noise can be calculated using the transfer function from $n_0(s)$ to $\Phi_{out}(s)$ with zero input phase:

$$\left(-\frac{\Phi_{out}(s)}{N} K_P F(s) + n_0(s) \right) \frac{K_V}{s} = \Phi_{out}(s);$$

$$\left(1 + \frac{K_P F(s) K_V}{Ns} \right) \Phi_{out}(s) = \frac{K_V}{s} n_0(s);$$

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{1}{s / K_V + K_P F(s) / N};$$

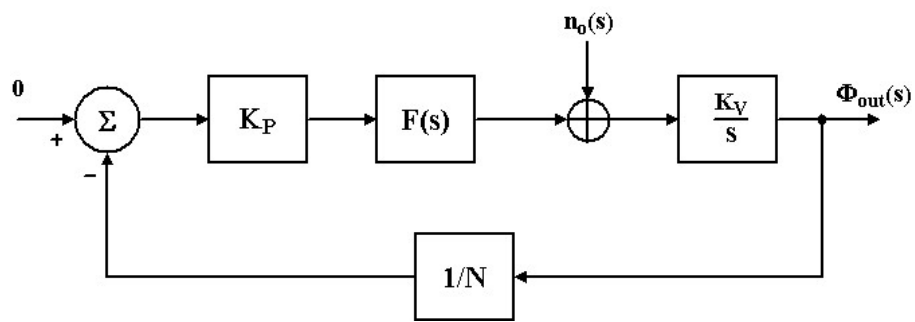


Figure B.3: Equivalent phase domain model of PLL with VCO noise source.

where K_V is in (rad/s/V). As shown in Eq. (1.6), $K_p \cdot F(s) = \frac{I_{CH}}{2\pi C_1} \cdot \frac{s\tau + 1}{s}$, therefore

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{1}{\frac{s}{K_V} + \frac{I_{CH}}{2\pi C_1 N} \frac{s\tau + 1}{s}} = \frac{2\pi C_1 N}{I_{CH}} \cdot \frac{s}{s^2 / \left(\frac{K_V I_{CH}}{2\pi C_1 N} \right) + \tau s + 1}$$

If K_V is in (Hz/V), the expression changes to

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{2\pi C_1 N}{I_{CH}} \cdot \frac{s}{s^2 / \left(\frac{K_V I_{CH}}{C_1 N} \right) + \tau s + 1} \quad (\text{B.24})$$

The power spectrum density of the output phase can be calculated by

$$\begin{aligned} S_{\Phi_{out}}(\omega) &= |n_0(j\omega)|^2 \left| \frac{2\pi C_1 N}{I_{CH}} \cdot \frac{j\omega}{-\omega^2 / \left(\frac{K_V I_{CH}}{C_1 N} \right) + j\omega\tau + 1} \right|^2 \\ &= \frac{N_0}{2} \cdot \frac{4\pi^2 C_1^2 N^2}{I_{CH}^2} \cdot \frac{\omega^2}{\left[1 - \omega^2 \cdot \left(\frac{C_1 N}{K_V I_{CH}} \right) \right]^2 + \omega^2 \tau^2} \end{aligned} \quad (\text{B.25})$$

where $N_0/2$ characterizes the power of the VCO input noise. As shown in Eq. (1.11), the loop bandwidth, $\omega_n = \sqrt{(K_V I_{CH})/(NC_1)}$, therefore,

$$S_{\Phi_{out}}(\omega) = \frac{N_0}{2} \cdot \frac{4\pi^2 C_1^2 N^2}{I_{CH}^2} \cdot \frac{\omega^2}{\left[1 - \left(\frac{\omega}{\omega_n} \right)^2 \right]^2 + \omega^2 \tau^2} \quad (\text{B.26})$$

Now assuming a noiseless VCO, the response of the loop to the phase variations in the input is evaluated. The input is usually generated by another oscillator, which will have its own phase noise characteristics. Considering the phase noise of $1/f^2$ region only, the input phase noise power spectrum can be given as $S_{\Phi_{in}}(\omega) = \alpha/\omega^2$, where α is a constant characterizing

the phase noise of the input oscillator. The equivalent phase domain PLL model for noisy input case is same as its transfer function model which is given in Eq. 1.8. Therefore, for the noisy input and noiseless VCO the output noise power spectrum can be given by

$$S_{\Phi_{out}}(\omega) = S_{\Phi_{in}}(\omega) \cdot |H(j\omega)|^2 = \frac{\alpha}{\omega^2} \left| \frac{1 + j\omega\tau}{1 + j\omega\tau - \omega^2 / \left(\frac{K_V I_{CH}}{NC_1} \right)} \right|^2 \quad (\text{B.27})$$

$$= \frac{\alpha}{\omega^2} \cdot \frac{\omega^2 \tau^2 + 1}{\left[1 - \omega^2 \cdot \left(\frac{C_1 N}{K_V I_{CH}} \right) \right]^2 + \omega^2 \tau^2}$$

Or if including the loop bandwidth,

$$S_{\Phi_{out}}(\omega) = \frac{\alpha}{\omega^2} \cdot \frac{\omega^2 \tau^2 + 1}{\left[1 - \left(\frac{\omega}{\omega_n} \right)^2 \right]^2 + \omega^2 \tau^2} \quad (\text{B.28})$$

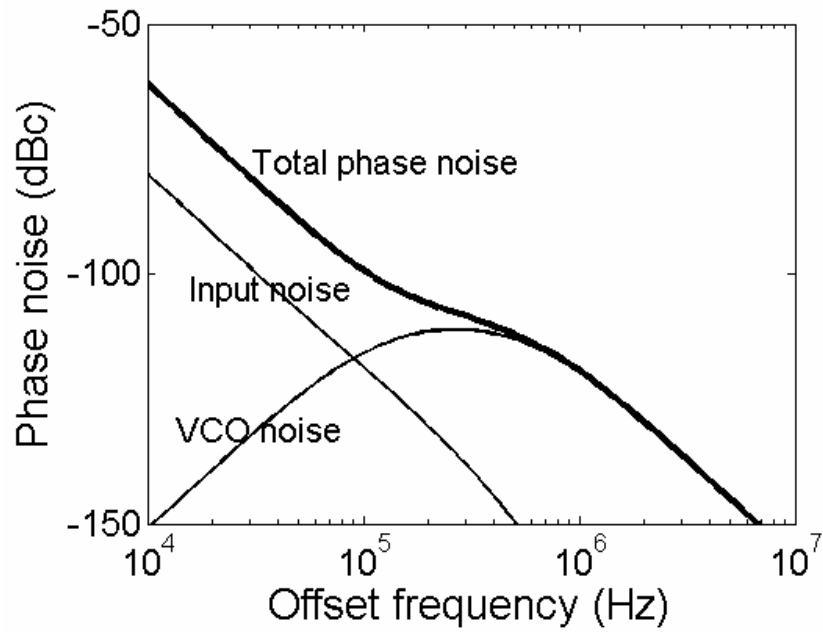
B.5 Discussion on PLL Phase Noise Based on Graphical Treatment

Superposition method is used on noise spectrum due to input noise, VCO noise and the divider noise to achieve the total PLL output phase noise. Simulation results are shown for different applications.

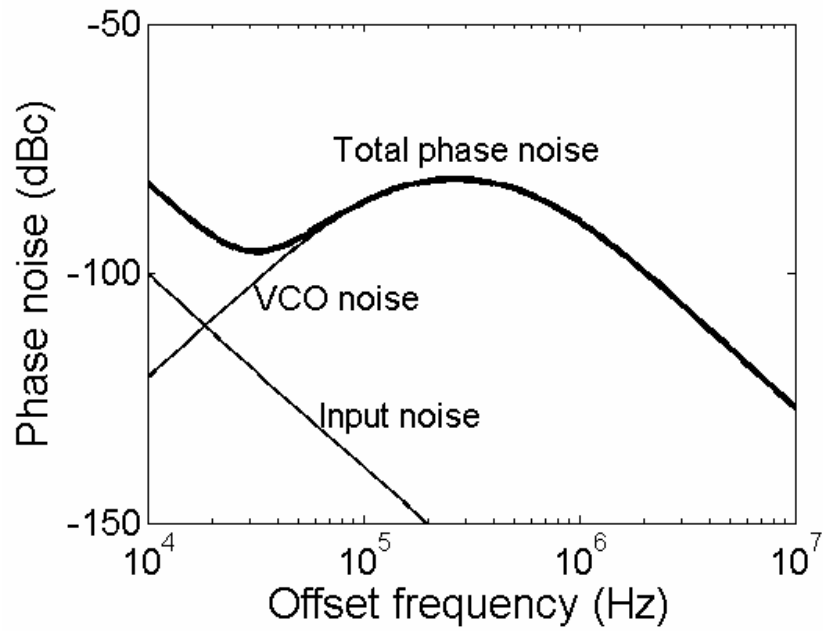
There are several important factors which affect the PLL output phase noise. Simulation results for different input noise, VCO noise, loop bandwidth and loop filter time constant are shown in Figs. B.4 to B.6, assuming the oscillation frequency is 100 MHz and the divider ratio is 8 for all the cases.

Figures B.4 (a) and (b) demonstrate the total phase noise when input noise is dominant and when the VCO noise is dominant. For the input reference noise dominant case, the total phase noise approximately equal to the input noise plus $20\log(N)$ at lower offset frequency. For

the VCO noise dominant case, the total phase noise has a peak occurring at the loop bandwidth frequency. Figure B.5 shows the total phase noise for different loop bandwidth. The peak position of the phase noise curve follows the loop bandwidth frequency. Moreover, phase noise curve with a lower loop bandwidth has a narrower peak. For higher loop bandwidth the curve is kind of flatten out with a wider shape. Figure B.6 shows total phase noise with different loop filter time constant, $\tau = RC_1$. A higher time constant gives a more flatten shape of phase noise curve.



(a)



(b)

Figure B.4: Simulation results of PLL phase noise for (a) input noise dominant, (b) VCO noise dominant.

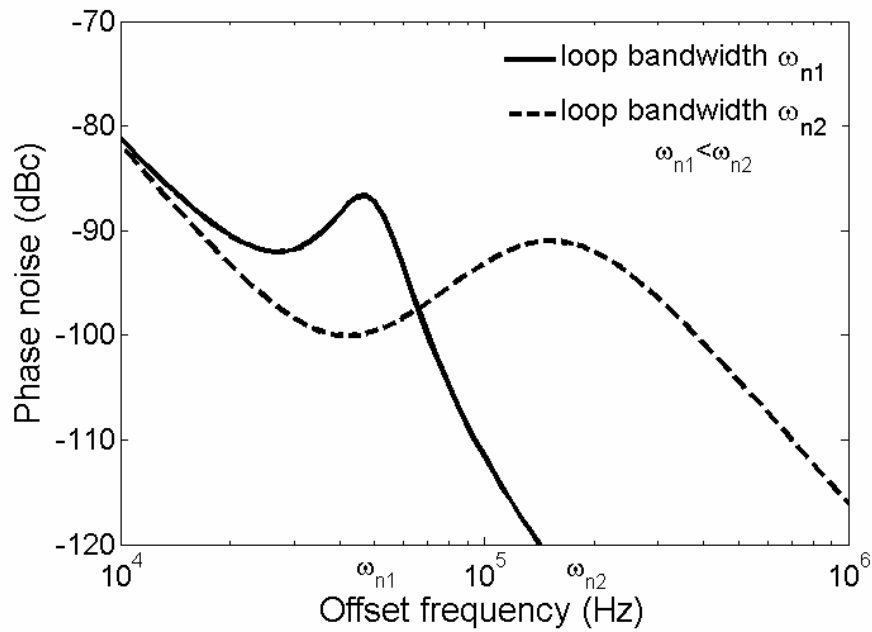


Figure B.5: Simulation results of PLL phase noise for different loop bandwidth.

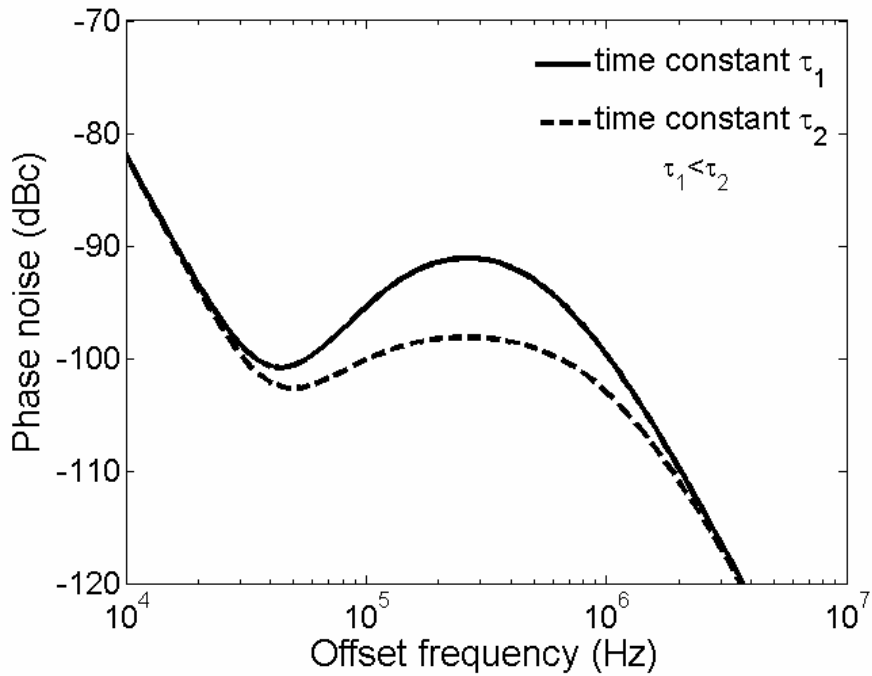


Figure B.6: Simulation results of PLL phase noise for different loop filter time constant.

APPENDIX C

LIST OF PUBLICATIONS

- C. Zhang and A. Srivastava, "Hot carrier effects on jitter performance in CMOS voltage-controlled oscillators," *Fluctuations and Noise Letters*, Vol. 6, No. 3, L329-L334, 2006.
- C. Zhang, A. Srivastava and C. Ni, "An experimental study on phase noise in phase-locked loops considering different noise sources," *Analog Integrated Circuits and Signal Processing*, under review, 2006.
- C. Zhang and A. Srivastava, "Hot carrier effects on jitter and phase noise in CMOS voltage-controlled oscillators," *Proceedings of SPIE – Noise in Devices and Circuits III*, vol. 5844, pp. 52-62, May 2005.
- C. Zhang, A. Srivastava and H. -C. Wu, "Hot-electron induced effects on noise and jitter in submicron CMOS phase-locked loop circuits," *Proc. of IEEE 48th International Midwest Symposium on Circuits and Systems (MWSCAS05)*, pp. 507-510, 2005.
- C. Zhang, A. Srivastava and C. Ni, "An experimental study on phase noise in phase-locked loops considering different noise sources," *Proc. of IEEE 49th International Midwest Symposium on Circuits and Systems (MWSCAS06)*, August 2006. Selected as one of the 12 finalists in Student Paper Contest (SPC).
- C. Salimath, C. Zhang and A. Srivastava, "Impact of Q-factor of an on-chip integrated inductor on the phase noise performance of a CMOS LC VCO based phase-locked loops," *The 7th Louisiana Materials and Emerging Technologies Conference*, Louisiana State University, Baton Rouge, Oct. 23-24, 2006. (poster paper).
- S. Herlekar, C. Zhang, H. -C. Wu and A. Srivastava, "Phase noise analysis for OFDM systems based on Hot-carrier effects in synchronization electronics," *Proceedings of SPIE - Noise in Communication Systems*, vol. 5847, pp. 150-159, May 2005.
- S. Herlekar, H. -C. Wu, C. Zhang and A. Srivastava, "OFDM performance analysis in the presence of synchronization errors induced by Hot-carriers," *Proceedings of 62nd IEEE Vehicular Technology Conference (VTC)*, vol. 3, pp. 1844-1848, September 2005.
- S. Herlekar, H. -C. Wu, C. Zhang and A. Srivastava, "Phase noise analysis for ICI self-cancellation coded OFDM with short-channel synchronization devices," *Proceedings of the IEEE Global Telecommunications Conference (GLOBECOM)*, vol. 1, pp. 230-234, 2005.
- S. Herlekar, C. Zhang, H. -C. Wu, A. Srivastava and Y. Wu, "OFDM performance analysis in the phase noise arising from the hot-carrier effect," *IEEE Trans. on Consumer Electronics*, vol. 52, no. 3, pp. 757-765, August 2006.

APPENDIX D

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Dear Editor,

My name is Chi Zhang. I am completing a doctoral dissertation at Louisiana State University titled "A study of phase noise and jitter in submicron CMOS phase-locked loop circuits." I would like to request your permission to include figures 3 - 5 and some content (text) belonging to sections 1 - 5 from one of my published works in my dissertation document. The title, volume number and publication date of this publication is as included below:

C. Zhang and A. Srivastava, "Hot carrier effects on jitter performance in CMOS voltage-controlled oscillators," *Fluctuations and Noise Letters*, Vol. 6, No. 3, L329-L334, 2006.

Your immediate response for this request will be highly appreciated as I am in the process of compiling the final document.

Thanks and regards,

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VITA

Chi Zhang was born on September 23, 1979, in Beijing, China. He received his Bachelor of Science degree in Electronic Engineering from Tsinghua University, Beijing, China, in July 2002. He has been enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, since August 2002 to pursue his doctoral studies. During this period, he received his Master of Science degree in Electrical Engineering in Louisiana State University, in December, 2003. His research interests include design and noise analysis of phase-locked loop (PLL) circuits.