

**CONTACT EFFECTS IN THERMALLY EVAPORATED
PENTACENE THIN FILMS AND ASPECTS OF
MIRCROSYSTEM HYBRID INTEGRATION**

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To my parents...

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ABSTRACT

Organic thin film transistors have the potential to replace silicon based transistors in applications such as smart cards and RF-ID due to their low cost and low processing temperatures. Thermally evaporated pentacene is studied as an organic thin film material. Thin film transistors were fabricated in bottom contact structure using thermal evaporation of pentacene at a rate of 0.5 to 1 nm/s. Heavily doped Si was used as a gate material and 100 nm thick silicon dioxide was used as a dielectric. Ni was used as contact metal for source and drain contacts. Threshold voltage of 16 V and mobility of 0.0016 cm²/V-s were obtained. Grain size in pentacene films increased from 120 nm to 150 nm upon annealing at 200 °C for 30 min. in nitrogen ambient. Resistivity of the pentacene films decreased with annealing temperature indicating an activation energy of 0.22 eV.

Hybrid Integration of a Bio-implantable Electrical Stimulation System (BESS) is carried out in the second part of this work. BESS produces periodic pulses that stimulate the gastric muscles. BESS consists of an application specific integrated circuit powered by rechargeable batteries, which are charged by a remote power delivery system. Screen printing technique was used for BESS hybrid integration. The same can be extended in future for fabricating organic transistors. The optimum screen printing process determined included squeegee speed of 2.2 cm/s, off-contact height of 2 mm and squeegee pressure of 80 PSI for ED3000 ink used. Ceramic, silicon, glass, polyimide and kapton substrates have been utilized for printing. Interconnect pattern of area 1" × 0.75" was screen printed on a ceramic substrate using ED3000 silver conductive ink and surface mount components were mounted. Bio-compatible 100 μm thick polyimide substrates were prepared by spin coating pyralin at 750 RPM and baked at 350 °C for 30

min. ED3000 conductive ink was used to print electrodes on polyimide substrates. The BESS system is now ready for full hybrid integration and testing.

1. INTRODUCTION

1.1 Need for Current Work

Silicon is one of the most abundant elements on the earth and is a central material in today's microelectronics industry. Since the invention of integrated circuits (ICs) in 1958, silicon based circuits have created a revolution in technology and transformed the modern lifestyle. Silicon field effect transistors (FETs) are used in large scale integrated circuits and memory chips. ICs today contain millions of transistors and are available cheaply. However, silicon also suffers from disadvantages which are inherent to its material properties or fabrication procedure. Some of these are listed below.

1. Fabrication of silicon ICs requires investment of billions of dollars in a fabrication line. The cost has to be amortized over a large volume of products. Hence, it is generally economical only for large scale production. Silicon devices have relatively high switching speeds. However, a) in areas where switching speed is not an important criterion, like in RF ID tags, memory cards or smart cards, or b) when the quantity needed is limited, or c) the product has a limited lifetime, for example in a single use disposable product; use of silicon may not necessarily be an economical choice.
2. Silicon is an indirect bandgap material which makes it unsuitable for many optoelectronic applications such as lasers and light emitting diodes.
3. Due to high temperature fabrication process of silicon ICs, integration with other passive components and microstructures is difficult. A new integration process needs to be developed utilizing pre-, co- or post-IC fabrication techniques [1].

Use of amorphous silicon avoids costs associated with making single crystal silicon and is suitable for fabricating low cost solar cells, smart tags and inventory control tags. However, amorphous silicon is usually deposited on a glass substrate [2].

Recently, a new class of semiconducting materials namely organic polymers are being investigated for specific applications. These new materials are inexpensive, can be processed at low temperatures and can be deposited on flexible substrates. This opens up new vistas in the development of cheap, flexible, large area electronics on paper-like flexible substrates such as fabrics and foils [3].

Organic materials have been used to make rectifiers, electro-optic switches, light emitting diodes, photo detectors, sensors and thin film transistors [4, 5, 6]. These new materials are inexpensive and the devices and circuits are also fabricated by inexpensive low temperature processes. Organic polymers not only offer a possibility of fabricating a range of existing electron devices, but also provide an opportunity to fabricate novel devices and extend the applications of existing inorganic semiconducting devices.

Organic devices can be fabricated by various inexpensive techniques including screen printing, ink-jet printing, spin casting and self-assembly techniques [7, 8, 9]. The availability of conductive and insulating polymers has made possible all-organic integrated circuits [10]. The all-organic circuit performance is approaching that of amorphous silicon devices. Organic devices are lighter, more robust and have enormous potential in the electro-optics industry and large area circuits.

The conductivity in organic polymers can be modified by controlling the polymer chain length during polymerization reactions. They can also be doped to increase conductivity. Higher carrier mobilities are being reported in transistors made of organic

materials, and their performance is now at a point where it competes with amorphous silicon [11]. Extensive research has begun on organic light emitting device (LED) based display and they are now commercially available in the market [12]. Organic LEDs emit a variety of colors and can be fabricated on flexible substrates enabling the development of robust flexible displays for applications like portable computers. There has been a growing research effort in this field to improve the semiconducting, conducting, and light-emitting properties of organic materials and improving organic-inorganic hybrid composites through synthesis and self assembly techniques [13].

Organic thin film transistors fabricated by using a screen printing process on a flexible substrate and integrated with passive components like capacitors and resistors, would realize organic printed circuit boards for roll-up displays. Hybrid circuits with organic thin film transistors and passive components can be fabricated at temperatures below 100 °C. Hybrid technology offers versatile interconnection technology to combine semiconductor devices and ICs with passive and distributed components which are difficult or impossible to fabricate on a chip.

Hybrid integration offers several advantages over discrete circuit boards. These include miniaturization that leads to reduction of size and weight, increase in component density, improvement in reliability by reducing soldering joints, reduction in packaging cost and simplified assembly and processing techniques.

In hybrid integration, interconnection pattern is screen printed using a conductive paste on a flexible or a ceramic substrate. Passive components like resistors and capacitors may also be screen printed or mounted on the substrate. IC chips may also be mounted on the substrate. With organic circuitry replacing the silicon based circuits in

electro-optics and smart cards, organic transistors along with resistors and conducting interconnect pattern can all be screen printed in fewer steps utilizing a simpler process.

Although organic thin film transistors may not encroach on the silicon FET market due to their inherent speed limitations, they can potentially replace them in large area circuitry where cost is a consideration and performance is not at a premium. The advantage of organic devices is that they offer a possibility of using a wide variety of semiconducting and insulating materials in combinations to address a variety of applications. Further studies are necessary to find suitable organic active materials with better properties, higher on/off current ratio, low leakage current and to optimize techniques used to fabricate organic devices so as to have improved carrier mobilities. Models for charge conduction in FET devices and contact resistance of the active layer/metal contact at the source and drain ends need to be further investigated for applications of organic thin film transistors to be commercially successful.

1.2 Research Goals

This work is divided into two parts. First, thermally evaporated pentacene is studied as an organic semiconductor for thin film FETs. Models for charge conduction in pentacene are discussed. Contact resistance between pentacene active layer and metal contacts are examined. Nickel is used as a metal contact. Hybrid integration, which is the focus of the second part of the thesis, can be employed for thin film organic circuitry.

In the second part of this thesis, hybrid technology is utilized to integrate and package a Bio-implantable Electrical Stimulation System (BESS) being developed in our laboratory. The central part of the BESS is an application specific integrated circuit which is powered by rechargeable batteries [14]. A remote power delivery system

(RPDS) is employed to charge these batteries [15, 16]. The BESS IC chip, the off-chip components, the batteries and the receiver coil circuit of the RPDS are all needed to fit inside the receiver coil which can be implanted inside the body. Since space is the biggest constraint in integrating this system, screen printing is used to replace the connecting wires, and miniaturized surface mountable discrete components are utilized. The circuitry with the IC chips and discrete components is mounted on a flexible substrate to be part of a bio-implantable microsystem. The output of the IC is carried to a set of electrodes that are printed on a flexible substrate also to be bio-implanted.

1.3 Organization of Thesis

Chapter 2 of this thesis gives the general background of organic field effect transistors and charge conduction principles. Chapter 3 gives experimental results of the thermally evaporated organic films, its current-voltage characteristics and contact resistance behavior. Chapter 4 deals with screen printing and hybrid integration of the BESS IC chip and chapter 5 gives the summary of the work done and suggestions for further work.

2. ORGANIC TRANSISTORS: BACKGROUND

Discovery of conducting properties of polymer polyacetylene in 1977 by Heeger, MacDiarmid, and Shirakawa, which later won them Nobel Prize in chemistry for year 2000, has paved way for this new field of organic electronics [17]. Organic transistors have the potential to replace silicon based transistors in applications where high switching speeds and high computational power are not needed. Organic transistors have cost advantage over silicon transistors due to low cost of materials and lower temperature processing. Organic polymers can be deposited by various methods including thermal evaporation in vacuum, molecular beam deposition, spin coating by using a precursor, organic vapor phase deposition and screen printing [7]. They can be fabricated on inexpensive large area flexible substrates such as paper or fabric-like plastic enabling their use in a variety of fields like communication, defense, optoelectronics and even consumer applications.

2.1 Organic Semiconducting Materials

A number of organic materials such as polythiophene, α -sexithiophene (α -6T) have been investigated for use in field effect transistors (FETs) [18]. Polycrystalline molecular solids such as α -sexithiophene (α -6T) or amorphous/semi-crystalline polymers such as polythiophene or acenes such as pentacene, teracene show the highest mobilities [19]. Figure 2.1 shows the evolution of organic materials and the improvement in their mobilities over the years [20]. Pentacene based FETs show the high mobilities and have been extensively studied. Pentacene is made up of five benzene rings as shown in Fig. 2.2 Pentacene has a sublimation temperature of 300 °C. Well ordered pentacene films can be deposited at low temperatures making it suitable for deposition on plastic substrates.

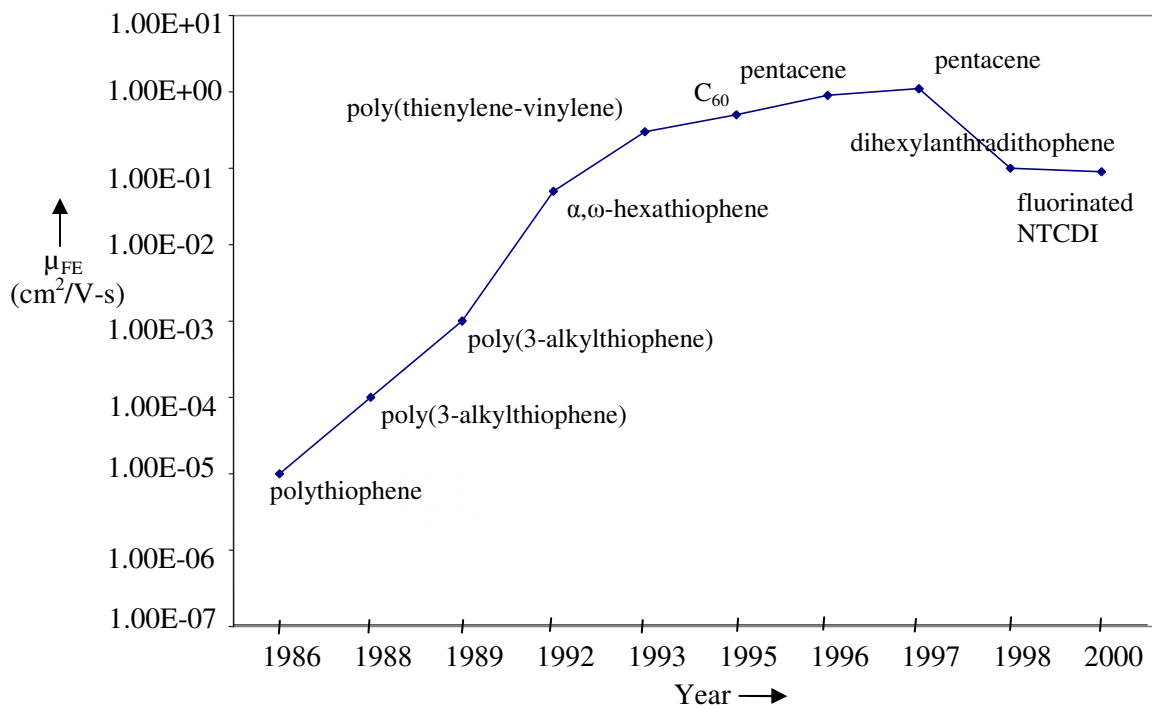


Fig. 2.1 Semilogarithmic plot of mobility vs. year. After reference [20].

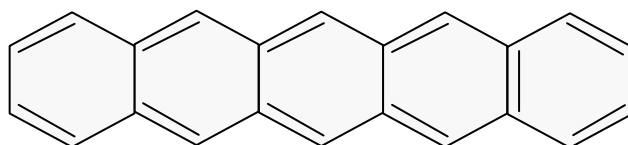


Fig. 2.2 Molecular structure of pentacene.

2.2 Conduction in Polymers

For a polymer to be electrically conductive, its electrons need to be free to move and not be bound to the atoms. The polymer should have alternate single and double bonds called conjugated double bonds. Carbon has six electrons distributed as $1s^2 2s^2 2p^2$, where the valence electrons in $2s^2 2p_x^1 2p_y^1$ orbitals form covalent bonds with neighboring carbon atoms of the polymer chain. Generally polymer chains have σ and Π double bonds. σ bonds are fixed and immobile and form a covalent bond between the sp^3 hybridized carbon atoms where one electron of the $2s$ orbital jumps into the p_z orbital. Π double bonds are formed in sp^2 hybridized carbon atoms, where the $2s^1 2p_x^1 2p_y^1 2p_z^1$ orbitals of the excited carbon atom form three σ bonds in one plane and a Π bond in a plane perpendicular to the σ bond. The electrons in conjugated Π double bonds are localized and not as strongly bound as the σ electrons. So the Π electrons can move rapidly along the chain especially under an applied electric field. Doping improves this movement by creating free electrons in a conjugated double bond through oxidation or reduction reactions [21].

Like silicon, whose electronic structure consists of conduction and valence bands formed due to a result of interaction between neighboring atoms, polymers too have overlapping molecular orbits which are occupied by the electrons of the sp^2 orbital. Using the quantum mechanical model for a free electron in a one dimensional box, the wave functions for the electrons of a polymer chain of N atoms separated by a distance of d is given by $E_n = n^2 h^2 / 8m(Nd)^2$, with $n = 1, 2, 3, \dots$ and where h is Planck's constant, m the electron mass and n a quantum number [21].

If the Π electrons from the p orbitals of the N atoms occupy these molecular orbits, with 2 electrons per orbit, then the highest occupied molecular orbit (HOMO) has an energy of $E(HOMO) = (N/2)^2 h^2 / 8m(Nd)^2$ and the lowest unoccupied molecular orbit (LUMO) will have an energy of $E(LUMO) = \left(\frac{N}{2} + 1\right)^2 h^2 / 8m(Nd)^2$. All energies are measured with respect to vacuum energy level as reference.

Thus, the energy required to excite an electron from the HOMO to LUMO is given by the difference between energy levels of LUMO and HOMO

$$\Delta E = (N + 1)h^2 / 8m(Nd)^2 \approx [h^2 / 8md^2] / N \text{ for large } N. \quad (2.1)$$

ΔE is the bandgap of that particular polymer and it is evident from Eq. (2.1) that the band gap is inversely proportional to the number of atoms N in the polymer chain. If the band gap is high, the material is an insulator and if it is low the material is a conductor. Usually semi-conducting polymers have a bandgap between 1.5 eV to 3 eV. Pentacene has energy bandgap of 2.5 eV, ionization potential of 5.1 eV for an electron in the HOMO level, relative dielectric constant of 4.0 and effective density of states of $5.8 \times 10^{21} \text{ cm}^{-3}$ [22]. Single crystal pentacene, deposited by slow thermal evaporation, is triclinic with unit cell parameters $a = 79.0 \text{ nm}$, $b = 0.606 \text{ nm}$, $c = 1.601 \text{ nm}$, $\alpha = 101.9^\circ$, $\beta = 112.6^\circ$, $\gamma = 85.8^\circ$. Plane spacing of (001) single crystal pentacene is calculated to be 1.449 nm [23].

2.3 Thin Film Transistors

Organic thin-film transistors contain a semiconducting organic layer which can be a polymer like polythiophene, α -6T or acenes like teracene or pentacene. An insulating polymer or silicon oxide or other insulator is utilized as a dielectric layer. The source and

drain contacts can be made from either a metal or a conducting polymer. The organic field effect transistors are fabricated in two configurations depending on how the source-drain contacts are formed on the structure. In the top contact structure shown in Fig. 2.3, the gate is deposited first on the substrate followed by the dielectric layer. The organic or the active material is deposited next followed by the source and drain metal contacts. In the bottom contact configuration shown in Fig. 2.4, the gate is first deposited on the substrate followed by the dielectric layer. The source and drain contacts are formed next

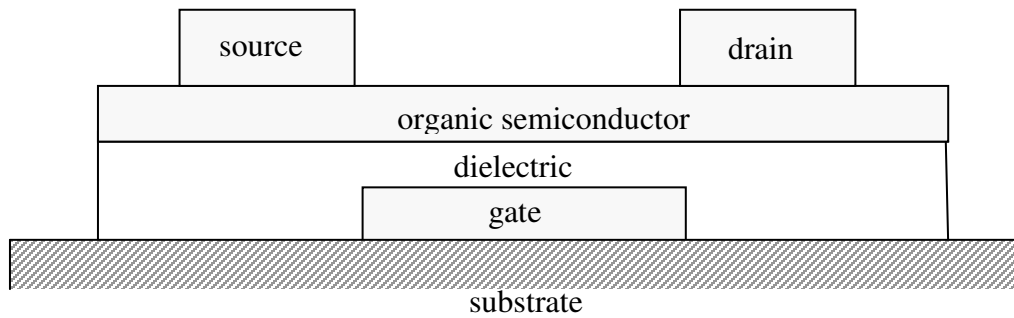


Fig. 2.3 Top contact structure.

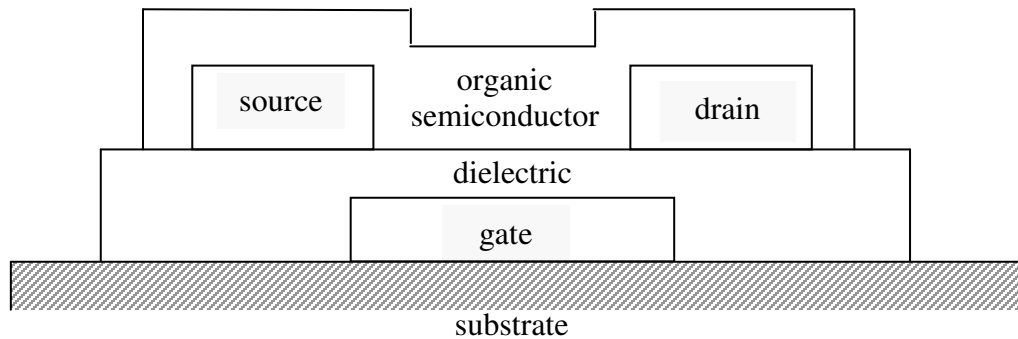


Fig. 2.4 Bottom contact structure.

followed by the active layer deposition last. In bottom contact configuration, the charge is laterally injected into the active layer from the source-drain contacts. In top contact configuration, the charge is injected vertically into the organic layer while the current flows laterally through the channel. The charge injection can be enhanced by doping the organic layer under the contacts.

Most of the organic materials commonly used for fabricating the field effect transistors are *p*-type. These devices operate in accumulation mode and usually have a positive threshold voltage. When the gate to source voltage is zero, the device is in ‘off’ state. Depending on the circuit operation, organic transistors conduct significant leakage current under applied drain to source voltage in the ‘off’ state. According to Rogers et al. [24] the bottom contact devices have low ‘off’ currents and better overall characteristics than the top contact devices. Pentacene consistently yields stable bottom contact devices with high current on/off ratio. Annealing reduces the ‘off’ currents significantly in these devices.

Vissenberg et al. [25] in their field effect mobility model for amorphous organic transistors showed that conductivity in organic transistors depends on the molecular ordering of the active layer. In highly ordered films deposited under vacuum, the *p*-type organic layer can be assumed as having a valence band and a conduction band. The charges are trapped in localized states and are released into extended state during transport. This transport depends on the temperature and applied gate voltage. In amorphous organic films, the transport takes place by hopping or thermally activated tunneling of carriers between the localized states. As the gate voltage is increased, the charges accumulated in the channel occupy the high energy states and require less

excitation energy to hop. This means that the mobility is dependent on the applied electric field.

The current through the channel in an organic FET is given by [26]

$$I_{on} = [W\mu_{FE} C_i V_D (V_G - V_T)]/L \text{ in linear region, and} \quad (2.2)$$

$$I_{on} = [W\mu_{FE} C_i (V_G - V_T)^2]/2L \text{ in saturation region.} \quad (2.3)$$

Here, W is channel width, L is channel length, μ_{FE} is the field effect mobility of holes, C_i is dielectric capacitance per unit area, and V_D, V_G and V_T are the drain to source, gate to source and the threshold voltages, respectively.

The ratio of ‘on’ current to ‘off’ current is given by [26]

$$I_{on}/I_{off} \approx \mu_{FE} C_i V_G / 2\mu_r \rho h \quad (2.4)$$

where μ_r and ρ are the mobility and density of residual charges and h is the height or thickness of the semi-conducting layer. The current on/off ratio depends on the field effect mobility μ_{FE} of the semiconductor, its thickness and its conductivity. The current conducted through the channel in an organic layer is directly proportional to the mobility of charge carriers in the film. The mobility of holes in polymers depends on the fabrication process involved and subsequent treatment of the deposited films. The mobility of carriers in pentacene based organic devices is dependent on the gate field and hence, termed as field effect mobility [27]. The field effect mobility can be increased by improving the molecular ordering of the deposited films and by purification techniques.

Organic FETs using thermally evaporated pentacene have shown high mobilities [11]. Annealing at high temperature increases the field effect mobility due to improvement in the molecular ordering of the pentacene layer. The molecular ordering of the evaporated pentacene films depends on the rate of thermal evaporation. Flash

evaporation results in poor molecular ordering and hence low field effect mobility values, while slow evaporation at a rate of 0.01 nm/s to 0.1 nm/s produces polycrystalline and crystalline films with high mobility values and low leakage currents. Bao et al. [28] have used screen printing technique to print organic poly(3-alkylthiophene) transistors on flexible substrates in which all layers including gate, dielectric, active, and source and drain were deposited using screen printing. The devices showed a mobility of 0.01 $\text{cm}^2/\text{V}\cdot\text{s}$. The channel length and width are limited by the resolution of the screen printer. Pentacene based devices have also been fabricated by screen printing technique by Gray et al. [29]. Here, the active layer was thermally evaporated on different dielectric materials like poly(vinylphenol), parylene and benzocyclobutene. Poly(vinylphenol) was spin coated, benzocyclobutene was screen printed and parylene was thermally evaporated. The performance of the FETs was investigated. The top contact devices with pentacene active layer, poly(vinylphenol) dielectric and gold source and drain contacts were found to have the best performance with mobilities near 0.3 $\text{cm}^2/\text{V}\cdot\text{s}$ and on/off current ratio between $10^3 - 10^4$. All-polymer integrated circuits have also been made by Drury et al. [30] by spin coating conductive polymers for gate, source and drain, insulating polymer for dielectric and semiconducting polymer precursor for an active layer. Screen printing of organic devices has its advantages over other fabrication techniques as the circuits can be simultaneously integrated with passive components on flexible substrates.

2.4 Metal Contacts and Other Factors

Li et al. [31] showed that the charge injected into a pentacene film depends on the schottky barrier between the source and drain metal contact and the active layer. The schottky barrier is dependent on the contacting metal and also the applied potential

between pentacene and metal. The work function of the contact metal affects the channel charge carrier density at the metal/active layer interface. For *p*-type pentacene, high work function metal results in high charge carrier density below the contacts and a low work function metal results in low carrier density below contact region. Metals that form a large schottky barrier with pentacene result in a large contact resistance between the source-drain and the active layer.

Since in the organic FETs, the source and drain regions are not usually doped, the charge carriers that form the conducting channel must be injected from the contacts. This charge injection is determined by the work function of the metal contacts through the schottky energy barrier.

Gold is the most preferred metal for use as source and drain contacts as its Fermi energy level is almost equal to the energy of the highest occupied molecular orbit leading to a low value for energy barrier to charge injection. Schroeder et al. [32] showed that threshold voltage and saturation current of a pentacene based thin film transistors with gold contacts varies with thickness of the active layer.

The mobility of carriers in organic materials is limited by the weak intermolecular interactions of the polymer chains and doping. Mobility of charge carriers within the chain of a polymer is high, but is limited by chain length. The high intra molecular mobilities can be taken advantage of by decreasing the channel length to the length of the polymer chain.

The mobility of carriers in organic devices depends on the surface roughness of the dielectric layers. Klauk et al. [33] used a variety of organic and inorganic dielectric layers like silicon dioxide, poly-4-vinylphenol (PVP) and poly-4-vinylphenol-co-2-

hydroxyethylmethacrylate (PVP copolymer) and found that the surface roughness of the dielectric layer affects the mobility of charge carriers in the active layer. Polymer dielectric layers have low surface energy as a result of better molecular ordering and high orbital overlap. They are smoother compared to silicon dioxide which leads to a higher value for field effect mobility for polymer dielectric layers. The actually value of mobility in field effect transistors will be lower than the value calculated from $\sqrt{I_D}$ vs V_G curves in saturation due to fringe current effects. The fringe current effects will be lower in transistors with W/L ratio higher than 10 [20]. An alternative approach to minimize fringe currents is to pattern the organic material such that the width of the active layer is the same as the width of the transistor. Mobility values in films deposited by spin coating solutions of organic materials are lower than the mobility values in thermally evaporated or chemical vapor deposited layers.

3. EXPERIMENTAL RESULTS ON THERMALLY EVAPORATED PENTACENE THIN FILMS

In this section, the results of resistivity measurements and contact effects in organic thin films are presented along with current-voltage measurements on organic FETs. Resistivity measurements on pentacene films deposited by thermal evaporation under vacuum and annealed under nitrogen at various temperatures are presented. The contact resistance at the metal/semiconductor interface is analyzed.

3.1 Experiment

Pentacene films were deposited on heavily doped *n*-type silicon substrates oxidized with 100 nm thick silicon dioxide layer. The wafers were cleaned in acetone followed by water and methanol rinses and dried in nitrogen before patterning. A positive photoresist S1813 from Shipley was spin coated on the silicon substrate at 2500 RPM for 50 seconds and exposed to UV light to transfer the contact pattern. A 150 nm nickel layer was then thermally evaporated on the patterned substrate and the photoresist was lifted off leaving 3 mm long and 1 mm wide nickel contact pads separated with a spacing of 50 μm , 75 μm , 100 μm and 250 μm . Pentacene was thermally evaporated onto the nickel contact patterns at 10^{-5} Torr. A charge of 25 mg of pentacene from Aldrich was used in evaporation boat. Typical film deposition rate of 0.5 – 1 nm/s was achieved. Figure 3.1 shows the plan view of the structure and Fig. 3.2 shows the cross sectional view of the device. The details of pentacene film deposition are given in the next section.

3.2 Pentacene Film Deposition

Pentacene of 98.8% purity is available commercially in amorphous form and has a sublimation temperature of approximately 300 °C. Twenty five mg of as-received

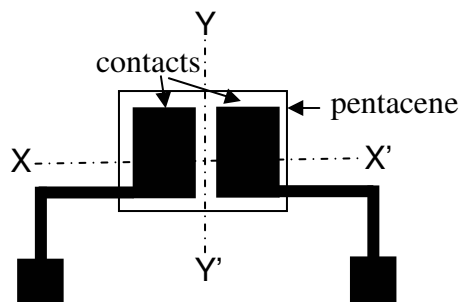


Fig. 3.1 Plan view of the organic FET structure.

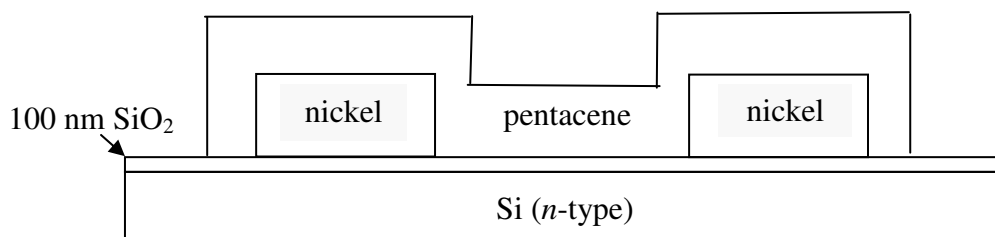


Fig. 3.2 Cross-sectional view of the contact structure along the line X-X' in Fig. 3.1.

pentacene was measured in a ceramic crucible and evaporated on the substrate through a shadow mask. Pentacene is sensitive to exposures to chemicals such as acetone which are commonly employed in photolithography. This makes it difficult to pattern pentacene films using standard photolithographic processes. Hence, a shadow mask is used to pattern the evaporated pentacene layer. The shadow mask employed in this work is a simple kapton film which is perforated in the areas where pentacene needs to be deposited. The mask can be peeled off the substrate after film deposition.

The vacuum chamber was pumped down to a pressure of less than 10^{-5} Torr and pentacene was sublimated at the rate of 0.5 – 1 nm/s. A ceramic crucible cleaned in methanol was used to hold pentacene, and a tungsten heating coil was used to heat the crucible. The substrates were kept at a distance of 10 cm above the pentacene source.

Figure 3.3 shows the schematic of the evaporation chamber. The average film thickness obtained was 130 nm as measured by Veeco optical interferometer. Figure 3.4 shows a typical measured thickness profile of a pentacene film when scanned along line X-X' and Y-Y' as shown in Fig. 3.1. The scan along X-X' (X - profile) gives the thickness of nickel contacts and scan along Y-Y' (Y - profile) gives the thickness of the pentacene film. After removing the shadow mask, the samples were annealed at temperatures of 100, 150 and 200 °C for 30 minutes under nitrogen ambient.

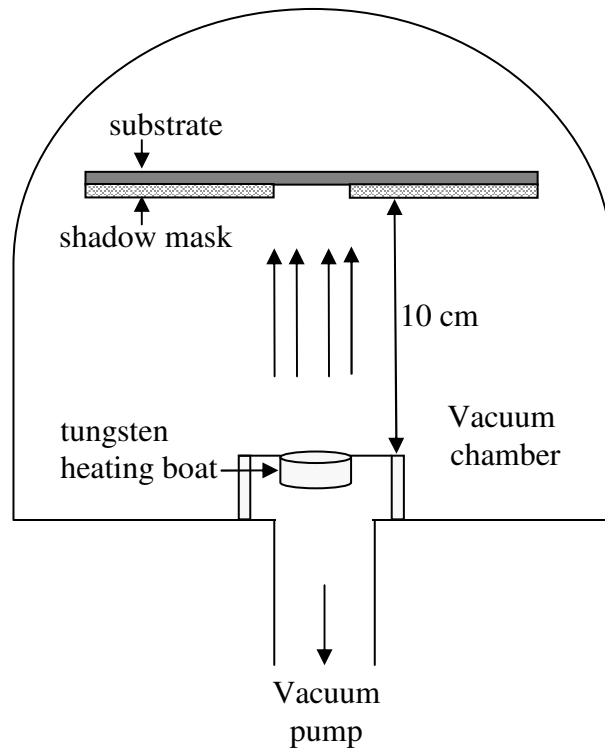


Fig. 3.3 Schematic of the evaporation chamber.

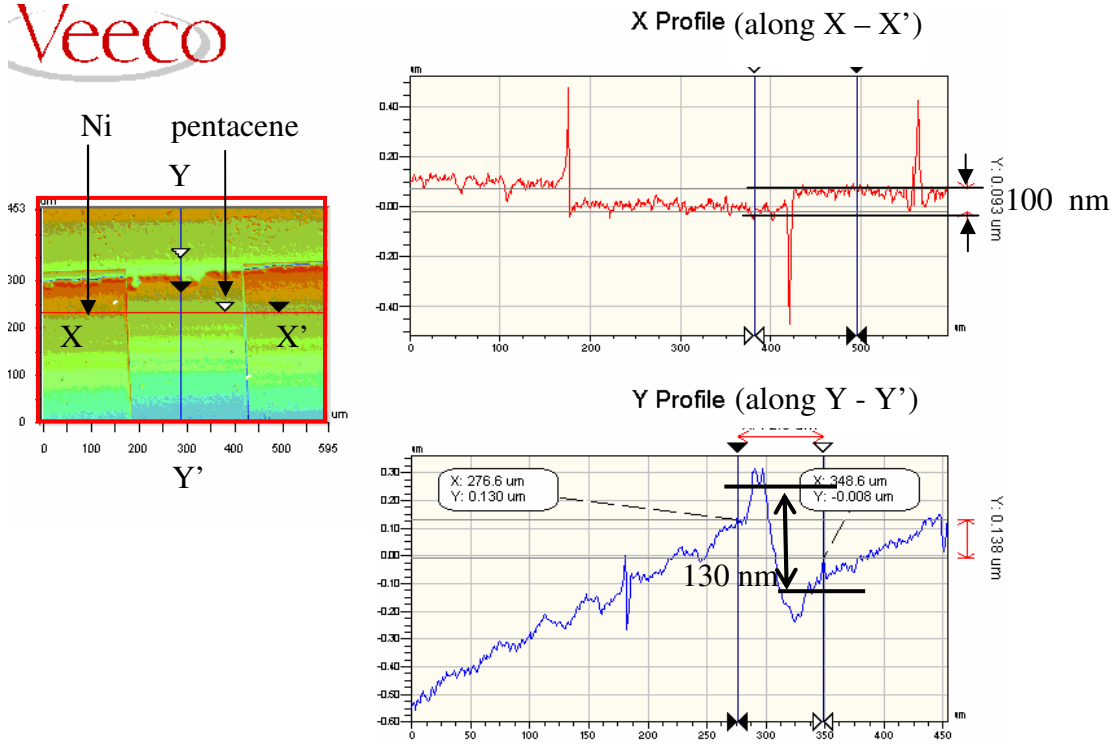


Fig. 3.4 Thickness profile of pentacene film and nickel contacts.

3.3 Resistance Measurements

The resistance of the evaporated pentacene film along with the contacts was measured by measuring the current passing through the film at a given voltage. A $1\text{ M}\Omega$ resistance is connected in series between the contact and ground and a voltage V_{DD} of 30 V is applied across the series combination as shown in Fig. 3.5. Resistivity ρ for the film is given by $\rho = R_p A/L$ where R_p is the pentacene film resistance, A is the cross sectional area and L is length. Now, $R_p = (V_{DD} - V_R)/I_D$, where $I_D = V_R/R$ is the current flowing through the structure. Here, V_R is the voltage across the external resistor.

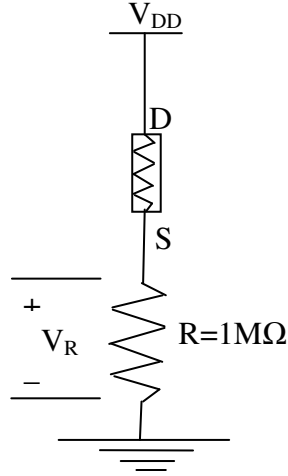


Fig. 3.5 Circuit for measuring current through the film.

The pentacene film resistivity ρ is hence given by:

$$\rho = \frac{(V_{DD} - V_R)Wh}{I_D L}. \quad (3.1)$$

Here, $A = W \times h$, where h is the thickness of the pentacene thin film and W is the width.

Room temperature resistivity of the pentacene films for different annealing temperatures as obtained from Eq. (3.1) is tabulated in Table 3.1. Figure 3.6 shows variation in room temperature resistivity of the evaporated pentacene films as a function of annealing temperature. As expected, the resistivity of the film decreases with annealing in nitrogen ambient. From Fig. 3.6, activation energy E_a of 0.22 eV is obtained using the equation for room temperature $\rho = \rho_o e^{-E_a/KT_a}$, where T_a is the annealing temperature.

Pentacene field effect transistors were fabricated in the bottom contact configuration shown in Fig. 2.4. A heavily doped n -type silicon substrate with 100 nm thick thermally grown silicon dioxide layer were used as the gate and the dielectric material, respectively. A 150 nm thick layer of nickel deposited on the oxide layer by

Table 3.1 Resistance R_p and resistivity ρ for pentacene films annealed at various temperatures under nitrogen ambient. $W = 3 \text{ mm}$, $L = 250 \text{ }\mu\text{m}$ $h = 130 \text{ nm}$.

Annealing Temperature ($^{\circ}\text{C}$)	V_{DD} (V)	V_R (V)	I_D (A)	R_P (Ω)	ρ ($\Omega\text{-cm}$)
No Anneal	30	30×10^{-6}	30×10^{-12}	10^{12}	1.5×10^6
100	30	90×10^{-6}	90×10^{-12}	3.33×10^{11}	0.5×10^6
150	30	200×10^{-6}	0.2×10^{-9}	1.5×10^{11}	0.27×10^6
200	30	600×10^{-6}	0.6×10^{-9}	5×10^{10}	90×10^3

thermal evaporation acts as source and drain. The back of the silicon substrate was etched in buffer oxide etchant to remove any oxide present. A 200 nm thick aluminum layer was deposited at the back of the silicon substrate. This layer acts as metal contact for the heavily doped n -silicon gate. Finally, pentacene was deposited on the source-drain contacts using a shadow mask, as described in the previous section. Figure 3.7 shows the cross sectional view of a pentacene FET and 3.8 shows the pentacene FETs fabricated in our lab. The FETs have a channel width W of 1 mm and length L of 250 μm . The W/L ratio is 4. Current-voltage characteristics of the FET were measured by connecting it as shown in Fig. 3.9. A 1 M Ω resistor was connected between the source and the ground, and a voltage V_{DD} was applied between the drain and ground. A negative voltage V_G is applied between the gate and the ground. The voltage V_R across the 1 M Ω resistance was measured to obtain the current through the device. Figure 3.10 shows the current-voltage

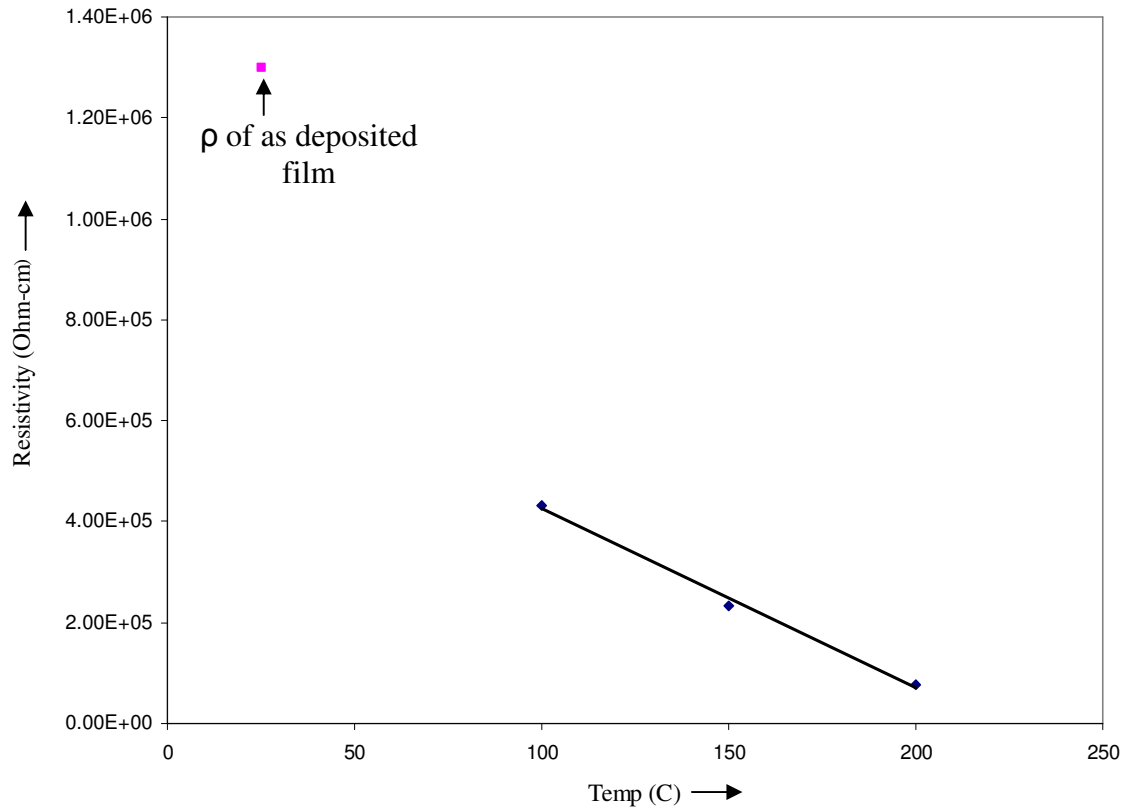


Fig. 3.6 Room temperature resistivity of pentacene films as a function of annealing temperature.

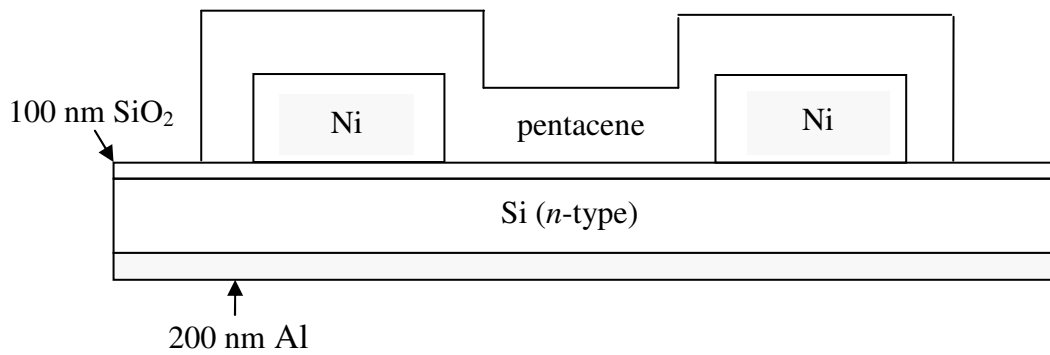


Fig. 3.7 Cross sectional view of the pentacene FET.

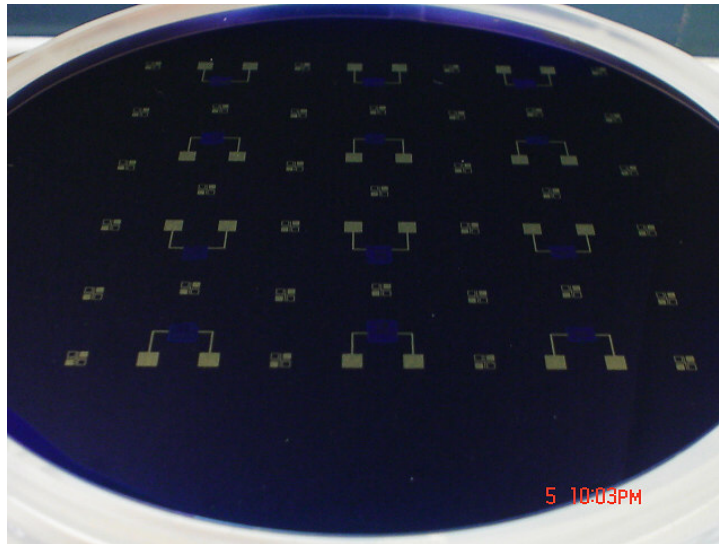


Fig. 3.8 Pentacene FETs fabricated on a silicon substrate.

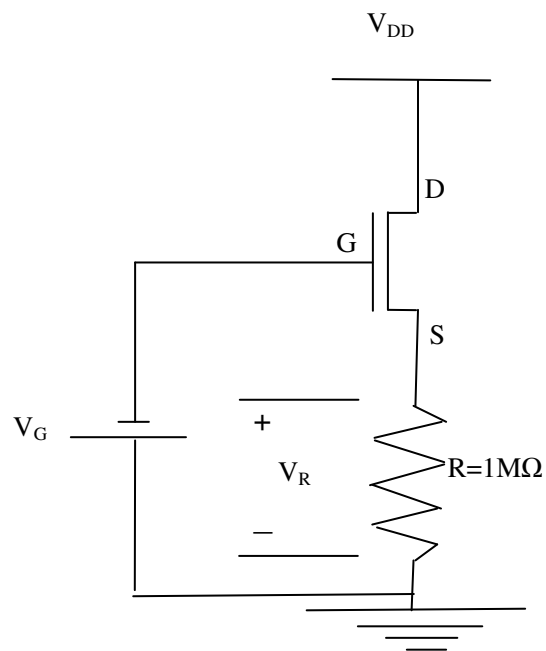


Fig. 3.9 Circuit for measurement of device current.

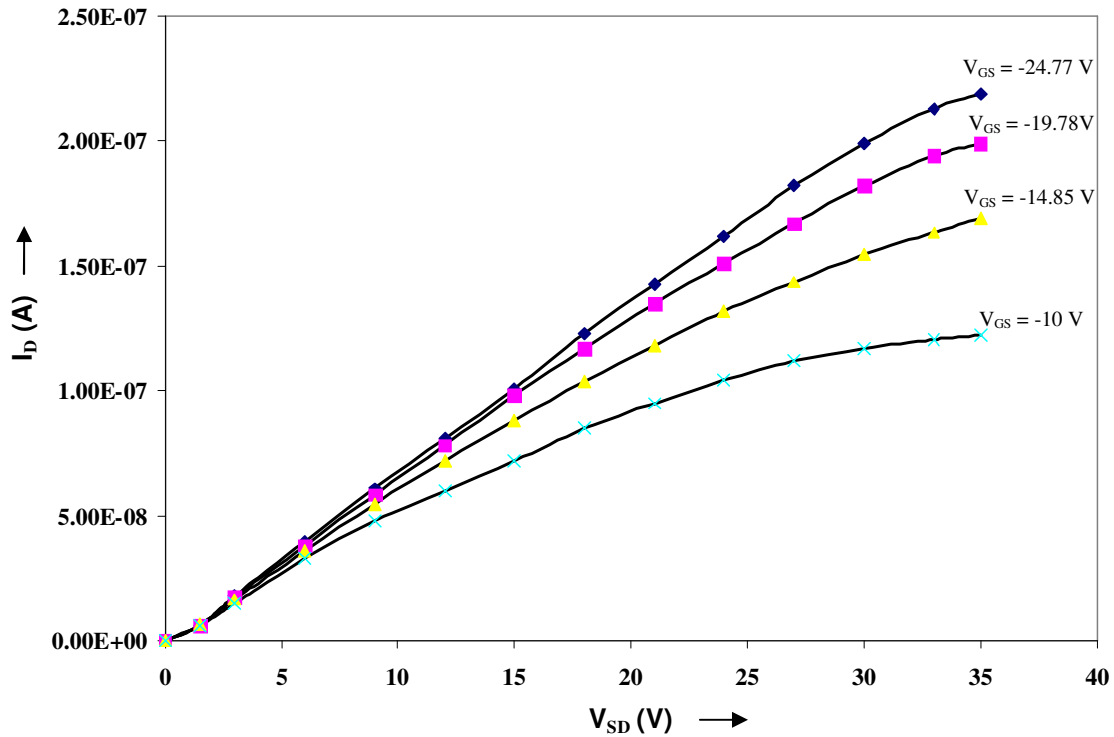


Fig. 3.10 I-V characteristics of pentacene FET with W/L ratio 4.

characteristics of the FET for different gate voltages. The pentacene layer on this FET was not annealed.

From Fig. 3.10, it is evident that the device tested here does not saturate. Higher source to drain voltages need to be applied for the device to saturate but the thickness of the oxide placed limitations on the maximum voltage that can be applied. The gate oxide is 100 nm thick and begins to break down as V_{GS} exceeds 35 volts. The devices were seen to be unstable. The current through the device varied with time and the variation did not appear to be systematic. This may be due to the gate-source and drain-source capacitors and the fringe currents due to the large contact areas of the source and drain contacts. The fringe current effect can be reduced by increasing the W/L ratio above 10.

Large W/L ratio pentacene FETs were also fabricated in this work. Using the process described above, FETs with W/L of 100, 200 and 400 were fabricated in the bottom contact configuration. The channel width was 1 cm and length was 25, 50, and 100 μm respectively. The deposition rate was kept much lower at 0.1 – 0.3 nm/s. The pentacene film was not annealed. Current-voltage characteristics were measured using the set up shown in Fig. 3.9. Figure 3.11 shows the variation of current with drain-source voltage for devices of various W/L ratios at zero gate to source voltage. When the gate to source voltage was varied from 0 to -30 V in steps of 10 V, the drain current did not vary. There was no gate control on the current through the device and the current was varying linearly with the drain-source voltage.

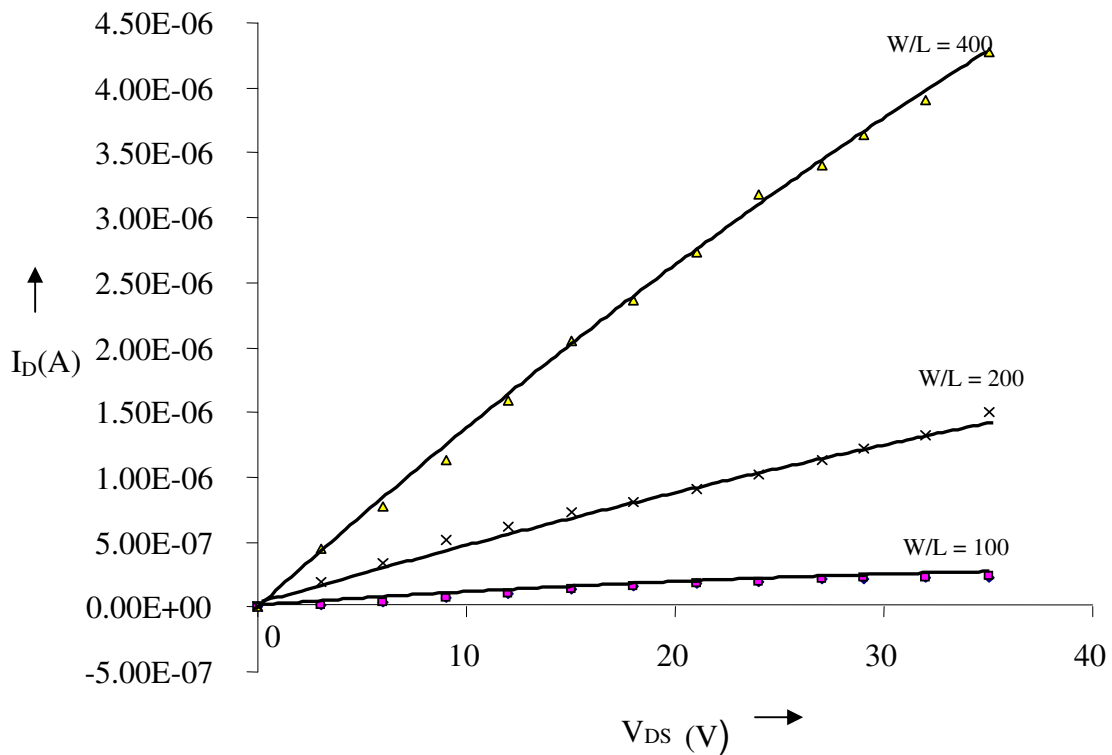


Fig. 3.11 Variation of current with drain-source voltage for W/L ratio of 100, 200 and 400.

3.4 Results and Discussions

Figure 3.10 shows the I-V characteristics of the pentacene FETs at various gate to source voltages. From the curves, threshold voltage of 16 V was obtained using Eq. (2.3). The channel width W is 1 mm and length L is 250 μm . The pentacene film was deposited at a rate of 0.5 – 1 nm/s. A positive threshold voltage means that the FET is ‘on’ under zero gate to source bias. The field effect mobility can be found by substituting the value of threshold voltage in Eq. (2.3). The Field effect mobility for device of W/L ratio 4 was found to be 0.0016 $\text{cm}^2/\text{V}\cdot\text{s}$. I-V characteristics of FETs of various W/L ratios were measured, but the current varied non-linearly with voltage and the FETs were seen to be unstable. This could be due to a) large non-linear contact resistance at the contacts, or b) small W/L ratio and large drain and source contact areas which result in fringing currents. The fringe current effects can be reduced by depositing pentacene only over the area between contacts, but use of shadow mask for pentacene deposition places a constraint on the deposition.

Large W/L ratio devices were fabricated to overcome the fringe current effects. Devices of W/L ratio 100, 200 and 400 with channel lengths of 25, 50, 75 and 100 μm and width of 1 cm were fabricated. The deposition rate was also much slower at 0.1 – 0.3 nm/s to obtain better ordered films. The devices I-V characteristics for various W/L ratios measured at zero gate to source bias are shown in Fig. 3.11. A threshold voltage of 1.5 V was obtained from the curves using Eq. (2.3) for a gate to source voltage of zero volts and W/L ratio of 400. This value however is not valid for any other gate to source voltage as the devices do not have any gate control. The field effect mobility obtained from the data is 0.009 $\text{cm}^2/\text{V}\cdot\text{s}$ for a W/L ratio of 400. The mobility of this device is higher than

the mobility of the device with W/L ratio of 4. This may be due to the slow deposition rate of the pentacene films in the former case leading to better molecular ordering.

3.4.1 Contact Resistance

The electrical characteristics of the organic thin film transistors in the linear region do not match the ideal MOS characteristics and these deviations are variously attributed to the contact resistance between the source/drain contact and the active layer. Sheshadri et al. [34] have measured the potential profile of organic devices and found that at any given value of source-drain voltage, most of the potential drop occurred at the source and drain contacts. The potential drop is not fixed but varies with the applied drain-source voltage and the drop at source-semiconductor interface is higher than the drop at drain-semiconductor interface. The threshold voltage, switching time and on-resistance of an organic FET are all degraded by this large effective contact resistance between the source/drain metal and the channel. This contact resistance can be attributed to various factors including the built in stress in the metal, interpenetration between the metal and the active layer, surface energy of metal leading to improper packing of organic molecules, schottky energy barrier between the metal and active layer, grain size and orientation of the film, device structures and presence of trap states at the interface. Therefore it is important to include the contact resistance in any FET model for determining current-voltage and threshold voltage characteristics.

Contact resistance depends on the work function of the metal used for contacts. Higher work function metals tend to create a stronger *p*-type region at the interface, while a low work function metal creates a depletion region in pentacene. The metal work function only affects the carrier density in the active layer surrounding the contact. At the

center of the device, between source and drain contacts, the channel carrier density is essentially independent of the drain and source metal contacts [31]. Li et al. showed that the work function of the gate material determines the channel carrier density in the active layer, given a fixed gate bias [31].

Burgi et al. [35] divided the channel into three regions with each offering different resistance to the charge carriers. The source to drain resistance R_{s-d} is given by $R_{s-d} = R_s + R_{ch} + R_d$ where R_s and R_d are the source and the drain contact resistances respectively. R_{ch} is the channel resistance. The source resistance can be written as $R_s = R_i + R_b$ where R_i denotes the effective resistance due to injection of charge carriers from the source. This resistance depends on the work function of the metal used for source and drain contacts. R_b is due to the bulk transport resistance near the contact where there is no accumulation region due to low carrier injection. Channel resistance is modulated by the gate voltage. For a p -type substrate, resistance associated with the drain contact is negligible as the contact is effectively forward biased by the drain voltage in the linear region. Hence, the entire resistance at the drain contact can be assumed to be due to bulk parasitic resistance. This contact resistance can be used to calculate the voltage drop V_C in the depletion region near the contact as in Street et al. [36] model for drain current as discussed below.

When the work function of the metal does not coincide with the energy of the highest occupied molecular orbit of the p -channel device or lowest unoccupied molecular orbit of the n -channel devices, a schottky barrier is formed between the metal and the active layer interface. It is the difference between the work function of the metal and the energy of the HOMO with respect to the vacuum level. The schottky energy barrier gives

a non-linear behavior for contact resistance. The schottky energy barrier depends on the work function of the metal used and can be lowered by gate potential. Higher the barrier, higher is the contact resistance. It appears that if the schottky energy barrier ϕ_B is below a critical energy barrier ϕ_B^* , then the channel current is limited by the mobility of carriers in the bulk region. If the barrier is higher than this critical barrier energy, the channel current is limited by the contact resistance [35]. The barrier energy ϕ_B depends on the metal and the organic semiconductor. For gold contacts to pentacene active layer, the barrier energy ϕ_B value is approximately 0.3 eV [32].

As shown in Figs. 2.3 - 2.4, two types of organic field effect transistors can be fabricated. The metal surface area in the contact with the active layer is small in the top contact geometry compared to that in the bottom contact structure. Though the channel carrier density is independent of the device type, the spatial variation of charge injection differs between the two device types. Street et al. [36] found that the output current-voltage (I-V) characteristics of the top contact structure follow ideal MOS characteristics that are linear at low drain-source voltages while that of the bottom contact structure current varies as V_D^β , where V_D is the drain to source voltage and β has a value in the range of 1.3 to 1.5. This deviation from normal characteristics has been modeled by dividing the channel into two regions. The voltage drop in the contact region closer to the source is V_C and the voltage drop in the main channel is $V_D - V_C$. According to their model, the channel current I_D is given by:

$$I_D = WC_G\mu[V_G - V_T - V(x)]\frac{dV}{dx}$$

where $V(x)$ is the channel potential, W is the channel width, C_G is the gate capacitance, μ is carrier mobility and V_T is the threshold voltage. Integration of above equation along the channel, except over the contact region which is assumed to be of length d , gives [36]

$$I_D = C_G \mu \frac{W}{(L-d)} \left[(V_G - V_T) V_D - V_D^2 / 2 - \left\{ (V_G - V_T) V_C - V_C^2 / 2 \right\} \right].$$

Assuming ohmic contacts, the voltage drop near the source V_C is given by $V_C = I_D R_C$

where R_C is the contact resistance.

3.4.2 Grain Orientation

The molecular ordering of the pentacene film depends on the surface on which the films are deposited. Pentacene is a non-polar molecule and repels any polar surface. When pentacene is deposited on a polar surface like silicon dioxide, pentacene molecules stand up almost vertically as shown in Fig. 3.12 and form a triclinic structure. Subsequent pentacene layers encounter different surface energy as they are being deposited on the pentacene ‘thin film’. Thus these layers are less ordered and have a smaller grain size and more trap states [37]. When pentacene is deposited on a metal surface, the back bone of the pentacene molecule is attracted to the metal leading to poor packing and poor molecular ordering as shown in Fig. 3.13, resulting in high resistance near the contacts. Although higher attraction between metal and deposited organic material leads to smoother films, this is not desired for pentacene thin films as attraction results in poor molecular ordering near the interface and decreased mobility due to scattering. The impurities that diffuse into the organic material during deposition may also act as dopants and trap charges, increasing the channel conductance and reducing the current on/off ratio.

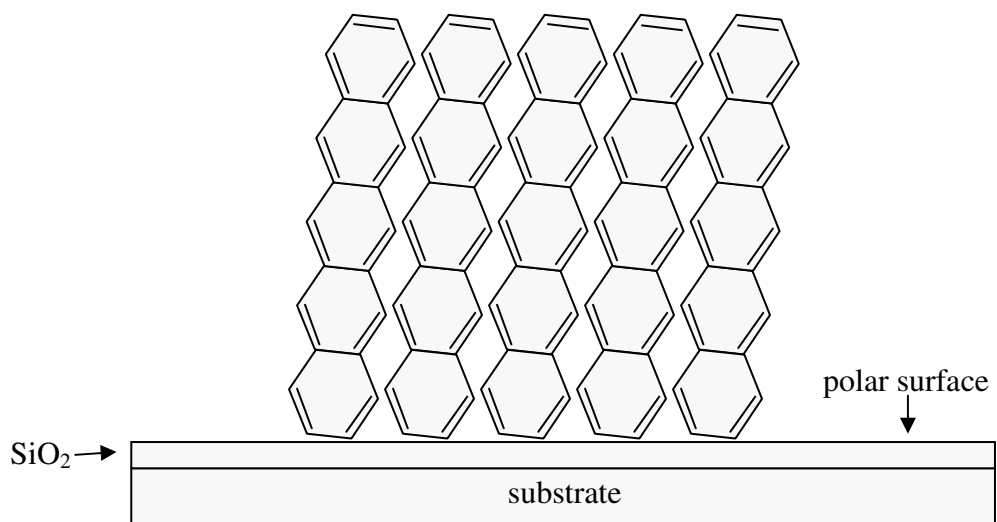


Fig. 3.12 Orientation of pentacene molecules on a polar surface.

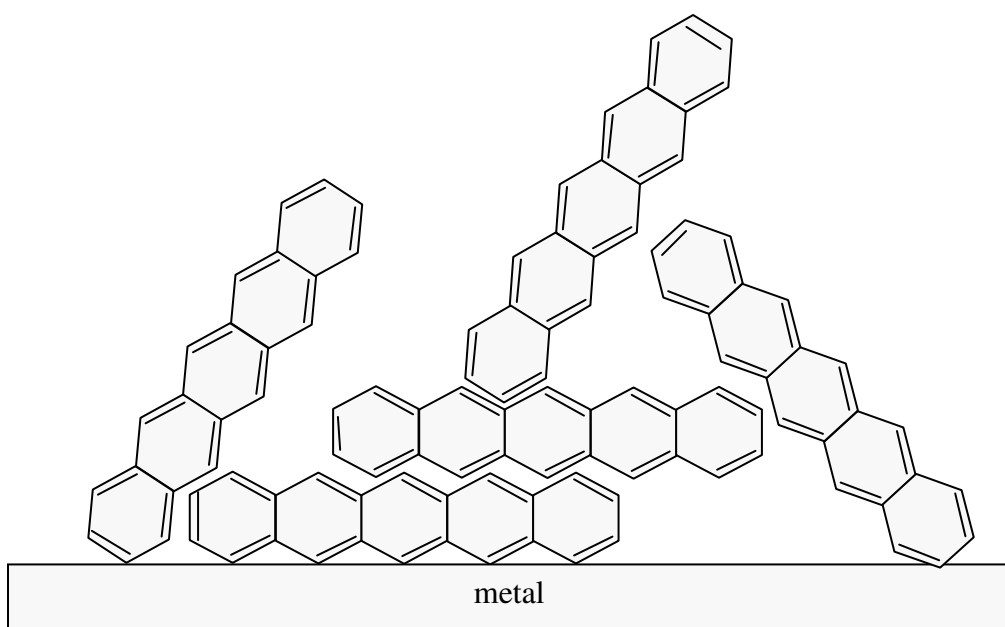


Fig. 3.13 Orientation of pentacene molecules on a metal surface.

The charge injection occurs only at the channel edge and hence the molecular ordering at the metal-active layer interface is important. Due to the difference in surface energies of metal and dielectric layers, the molecular ordering at the contact and near the center of the channel are different, with the center having more ordered layers. The molecular ordering near the contacts can be improved by employing proper surface treatment procedures. Care should be taken while deposition that no impurities are incorporated into the active layer. Impurities act as trap states which reduce carrier mobility. Treating dielectric surface with octadecyltrichlorosilane (OTS) will result in an increased grain size near the interface, thus improving the hole mobility at the pentacene OTS surface [38]. Slower deposition rate and higher annealing temperature can increase the grain size around metal contacts thereby reducing contact resistance. Watkins et al. [39] found that the behavior of metal-semiconductor interface depends on the contact metal used for source and drain. For gold and silver contacts, the behavior is asymmetric. The source interface behavior is different from that of the drain interface, with energy barrier being higher at source than at drain.

It is difficult to model for contact resistance in any device output I-V model as contact resistance depends on a variety of factors, some of which can be controlled and others which cannot be controlled. The contact resistance affects the level of carrier injection and threshold voltage and is difficult to quantify. However, the contact resistance can be decreased by suitable choice of metal which forms a lower schottky energy barrier with polymer film. The Fig. 3.14 shows the work functions of different metals and pentacene. Gold has the lowest schottky energy barrier with pentacene and is widely used. In the current work, Ni is used as contact material as it provides low

schottky barrier to pentacene as seen from the Fig. 3.14. E_{vac} in Fig. 3.14 indicates the vacuum level.

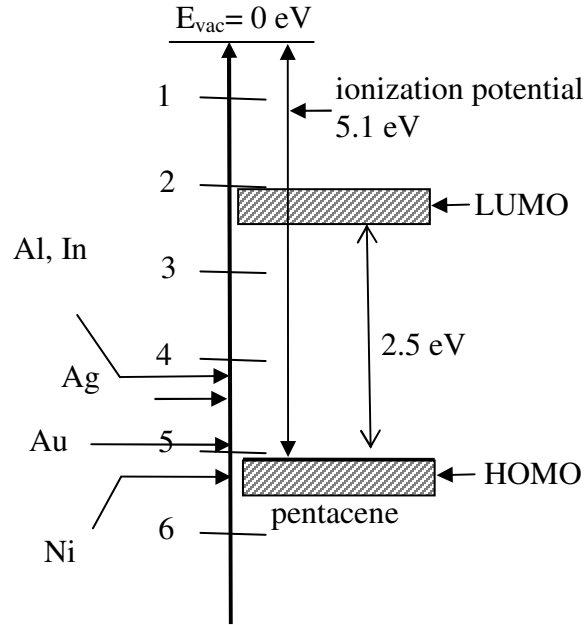


Fig. 3.14 Work function of various metals and ionization potential of pentacene.

3.4.3 Annealing of Films

Annealing pentacene films increases grain size and improves their molecular ordering. The resistivity of the films also decreases. Kang et al. [40] annealed pentacene films at temperatures of 50, 70 and 90 °C for 2 hours and found that the average grain size increased from 210 nm to 630 nm. In the current work, thermal evaporated pentacene films were annealed at 100, 150 and 200 °C in nitrogen ambient for 30 minutes. The resistivity of the films was measured and the results were presented in Table 3.1. The variation of resistivity as a function of temperature is shown in Fig. 3.6. The resistivity of the films decreases with annealing temperature. The surface of the films was scanned

using AFM. Figures 3.15 – 3.16 show the AFM images of pentacene films annealed at 200 °C. As can be seen from Fig. 3.15(a) and (b), the grain size of the annealed films is approximately 120 nm for room temperature film and 150 nm for annealed films at 200 °C in nitrogen ambient. The grain size of pentacene did not show any major increase after annealing. The increase in conductivity shows densification of the films and better molecular ordering. As the grain size increases, the charge carrier scattering decreases and field effect mobility increases. Annealing enhances mobility. Defects and misoriented crystallites are reduced by annealing. The defect activation energy of the films was found to be 0.22 eV. Figure 3.15 shows the height of the grains and Fig. 3.16 shows the 2-D view of the surface.

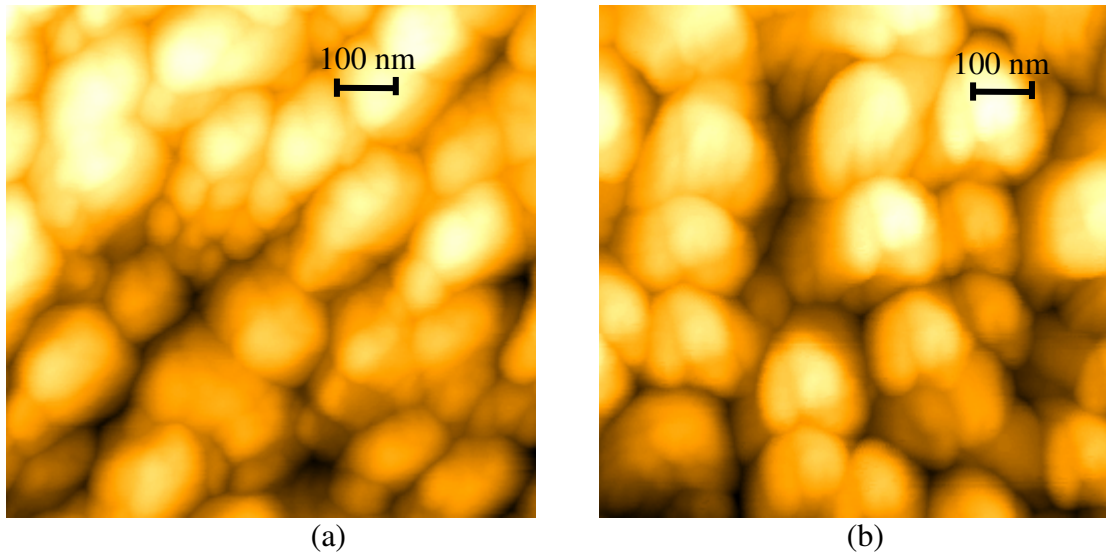


Fig. 3.15 (a) 'Height' profile of pentacene deposited at room temperature.
(b) 'Height' profile of pentacene deposited at room temperature and annealed at 200 °C in nitrogen ambient.

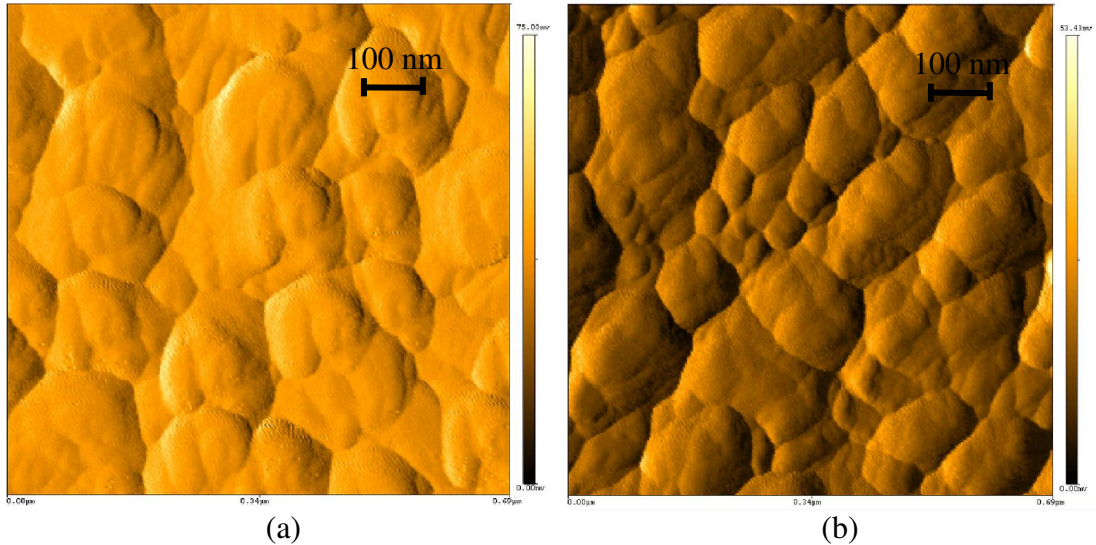


Fig. 3.16 (a) ‘Error’ profile of pentacene surface deposited at room temperature.
 (b) ‘Error’ profile of pentacene surface annealed at 200 °C under nitrogen ambient.

The large contact resistance at the metal-semiconductor interface and the schottky energy barrier can be lowered by selective doping of the pentacene film at the contacts. In top contact devices, the threshold voltage is a function of the thickness of the active layer. This is the result of an energy barrier that exists between the contacts and active layer.

3.5 Summary

Pentacene thin films were thermally evaporated at various deposition rates. Films with slower deposition rate of 0.1 – 0.3 nm/s were found to have high mobilities compared to films deposited at a faster rate of 0.5 – 1 nm/s. FETs of W/L ratio of 4 with channel length L of 250 µm and width W of 1 mm were fabricated in bottom contact configuration. Heavily doped *n*-Si was used as gate layer and 100 nm thick thermally grown silicon dioxide was used as gate dielectric layer. 150 nm thick thermal evaporated Ni was used as source and drain contact metal. Pentacene was thermally evaporated through a shadow mask. The active layer was deposited at a rate of 0.5 - 1 nm/s. The pentacene film thickness was 130 nm. Threshold voltage of the device was found to be 16

V and the field effect mobility was found to be $0.0016 \text{ cm}^2/\text{V}\cdot\text{s}$. Pentacene FETs of W/L ratio 100, 200 and 400 were also fabricated. Pentacene was deposited at a slower deposition rate of $0.1 - 0.3 \text{ nm/s}$. These devices do not have any gate control. The FETs have threshold voltage of 1.5 V and mobility of $0.009 \text{ cm}^2/\text{V}\cdot\text{s}$ for a gate to source voltage of zero volts. Pentacene films were deposited on Ni contacts and annealed at 100, 150 and $200 \text{ }^\circ\text{C}$ for 30 min. in nitrogen ambient. The resistivity of the films was measured and plotted against temperature. Defect activation energy of 0.22 eV was obtained. The grain size of the pentacene films was found to be 120 nm for a room temperature film and approximately 150 nm for films annealed at $200 \text{ }^\circ\text{C}$ for 30 min. in nitrogen ambient.

4. HYBRID INTEGRATED CIRCUITS

In this chapter, hybrid packaging of a Bio-implantable Electrical Stimulation System (BESS) is discussed. The parameters for screen printing an interconnect pattern for BESS chip, bio-implantable electrodes and hybrid packaging are discussed.

4.1 Introduction

Screen printing is one of the most convenient methods to fabricate reliable and cheap organic thin film transistors. Screen printing electronic circuits is developed from silk screening, the art of printing on cloth. Screen printing electronic circuits is a simple and often economical way to mount, interconnect and package circuit components on a common substrate. Printing electronic circuits involves forcing ink paste through a stencil or screen such that it deposits on the substrate in a delineated pattern. Circuits can be printed on rigid substrates like ceramic, glass and silicon or flexible substrates like kapton, polyimide and fabric. The ink pastes that are used for screen printing need curing. The ink curing temperatures can vary depending on its constituent ingredients. The capacitors, resistors and related circuitry for hybrid applications can be printed in relatively fewer steps. In this work, screen printing has been utilized for packaging a gastric pacer circuit.

The gastric pacer circuit or BESS consists of an application specific integrated circuit which generates electric pulses at a specific amplitude and frequency. These pulses are sent to a set of electrodes implanted in the body, and stimulate the gastric muscles [14]. The electrodes are screen printed here on a flexible implantable substrate. The IC is powered by a set of batteries which can be charged using a remote power delivery system (RPDS) consisting of a transmitter coil, a receiver coil and associated

circuitry [15, 16]. The IC, off-chip components and the receiver coil circuitry need to be integrated and packaged in 1" × 1" × 0.5" space such that it fits inside the receiver coil.

4.2 Background

The screen printing process needs three important components comprising of screen or mesh, thick-film paste or ink and substrate. These are described in the following sections.

4.2.1 Ink

The ink or paste is the most important component in screen printing process. The properties of the ink such as viscosity, homogeneity and rheological characteristics affect the thickness and quality of the print. Good line resolution can be obtained if the surface energy of the substrate is lower than the surface energy of the ink [41].

There are three categories of thick-film pastes or ink generally used in electronics industry. These are conductor, resistor and dielectric inks. Each paste normally contains three constituents namely metal or appropriate particles, vehicle and binder. The metal, for example can be silver, gold, platinum or a combination. The maximum particle size should be less than half the opening of the mesh, to facilitate free movement of particles through the open mesh areas. The vehicle is an organic solvent which evaporates during curing, leaving a mixture of glass frit and metal. The ink should be viscous enough not to flow through the open areas of the screen under no applied shear stress.

When the squeegee moves over the ink, a shear stress is applied and the viscosity, which is a function of shear stress, decreases, enabling the ink to flow through the open areas and settle on the substrate. Once the ink deposits on the substrate, it will regain its original viscosity (assuming Newtonian behavior) and levels itself. The squeegee

pressure should be sufficient enough to force the ink through the open areas. If the squeegee pressure is too high, the ink may change its property and transform into a non-Newtonian fluid and does not regain its viscosity. This results in ink spread across the substrate blurring the line definition. If the ink is too viscous, it does not flow through the open areas and if it is too thin, it spreads out resulting in a bad quality of print.

4.2.2 Substrate

The substrate is a mechanical base for the hybrid circuit and acts as an electrical insulating material. It is important to choose a proper substrate depending on the application, as it affects both the process used and final characteristics of the hybrid circuit. Some of the properties of the substrate that influence the print quality include 1) the coefficient of thermal expansion, 2) volume resistivity, 3) mechanical strength, 4) surface finish, and 5) surface energy.

Ceramic substrates are inexpensive and are easy to work with. Ceramics such as alumina, beryllia, magnesia are the most commonly used substrates in thick film printing. The purity and surface finish defines the type of films that can be printed on the substrates. For example, 96% pure alumina with a rough surface finish is used for printing thick films while 99.9% pure alumina with very smooth surface finish is used for thin film circuitry. Surface roughness affects the quality of print. A rough surface improves adhesion of ink to the substrate, but too rough a surface results in non-uniform print as some parts of the screen will not be in contact with the substrate during printing. Ceramic, glass, and silicon substrates are hard and have virtually no elastic deformation under high squeegee stress, while on the other hand kapton and polyimide substrates are flexible and deform under high stress.

4.2.3 Substrate Cleaning

Substrate cleaning is critical as it affects sticking between the wet ink and the substrate. Ceramic substrates in this work were cleaned in boiling trichloroethylene and stored in methanol till their use. Glass and silicon substrates were cleaned in acetone, water and methanol and dried with nitrogen.

4.2.4 Mesh Screen

A good mesh screen should have high tension and relaxing properties, longevity and good ink flow through the open areas. The latter influences thickness of print. Steel and polyester are two types of materials that are commonly used to make mesh screens. In this work, polyester mesh is used as it has all the properties required for printing electronic circuits and is cheaper compared to steel mesh. The mesh count gives the number of wires per inch of the screen. Important parameters that define the wet print thickness include the mesh count, the diameter of the wire, the percentage open area and the emulsion thickness [42]. Mesh is selected based on the feature size of the pattern. A mesh with thin wires and high mesh count is used to print fine features and thin print, while a mesh with thick wires will result in coarse, thick print. Higher open areas result in a thicker print.

4.2.5 Exposure

A screen needs to be patterned before printing is commenced. This is usually done by placing a mask over the area that needs to be imprinted on the screen and exposing it to UV light. The mask is generally made of a transparency contains the designed the art work. There should not be any air gap between the screen and the mask. This is achieved by using vacuum to hold the mask in place. Then, UV light is shone on the screen

exposing the emulsion. The masked areas which are unexposed dissolve in water when developed leaving open areas in the screen. Water is a common developer for screen emulsions.

4.2.6 Printing Process

The screen delineated with the desired pattern is mounted on the frame holder of the screen printer. The substrate is held on a leveled platform by vacuum and the off-contact height is adjusted using the four screws at four corners of the screen printer. The squeegee arm is moved to the extreme end of the screen and a small amount of ink is placed in front of it. The squeegee speed is adjusted using the pressure gauge, and the squeegee pressure is changed to apply the required amount of shear on the ink. When the squeegee moves over the screen, the viscosity of the ink decreases and it flows through the open area, and settles on the substrate as the screen peels off. Figure 4.1 shows the printing process steps. If the squeegee pressure is too high, the ink may spread and expand the delineated line width and if it is too low, the ink may not flow through the open areas. The squeegee speed also is important in obtaining continuous film.

The spacing between the screen and substrate is variable and this distance is known as off-contact height. When the screen is in direct contact with the substrate, it is called on-contact printing. The advantage of off-contact printing over on-contact printing is the snap-off action of the wire mesh. When the squeegee moves over the screen, the screen deflects and touches the substrate and the ink is flooded into the open areas of the screen. As the squeegee passes over these open areas, the screen deflects back to its original position due to the tensile stress in the mesh strings. This is called snap-off. The snap-off forces the ink to separate from the wire mesh openings and deposit on the

substrate. In contact printing there is no snapping of the screen and as a result some of the ink remains in the screen after the print stroke, resulting in either non-uniform or thinner print. Moreover, in on-contact printing, the screen is in contact with the ink even after the print stroke. This may expand the line width and hence fine resolution print is difficult.

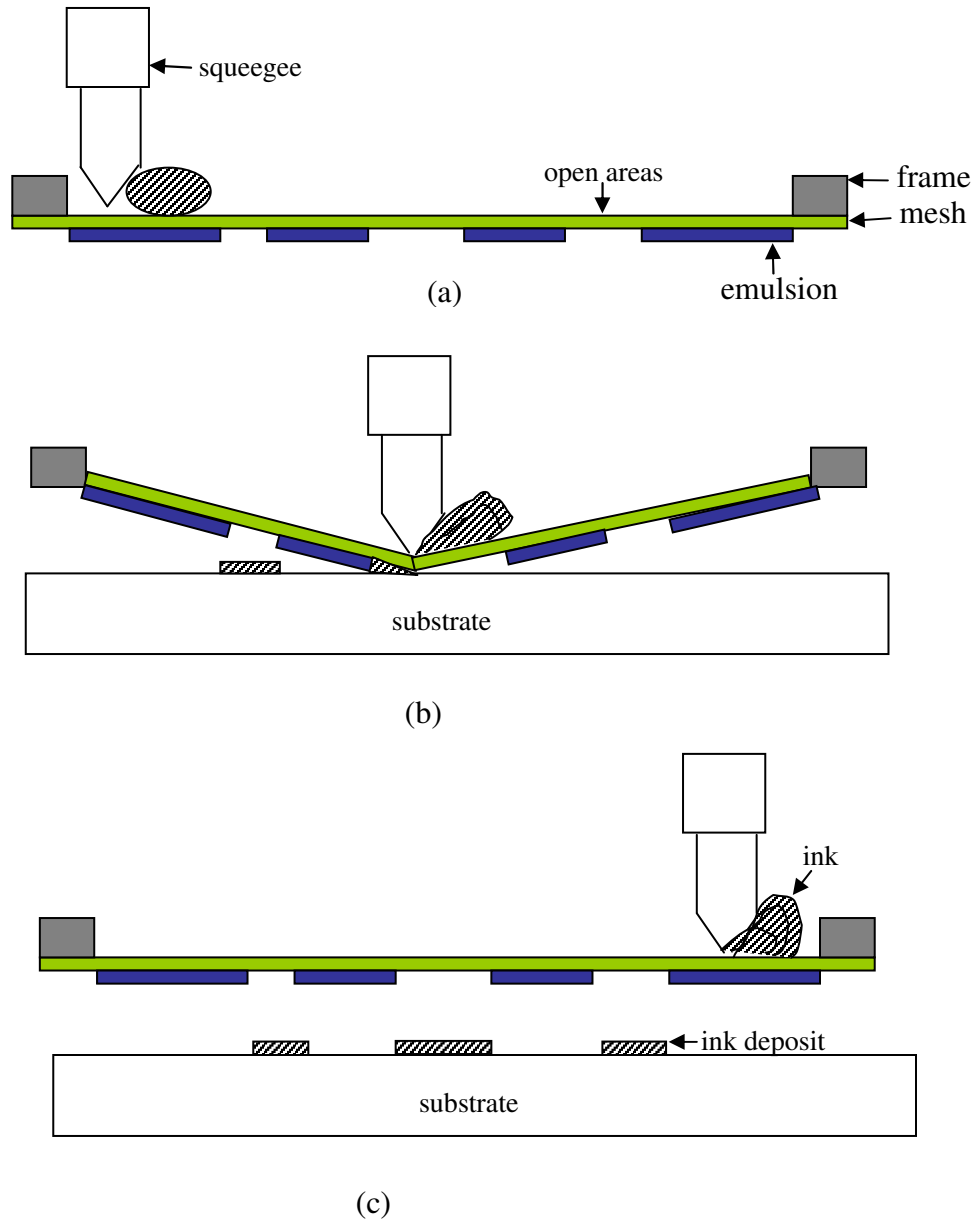


Fig. 4.1 Screen printing process (a) before printing, (b) during printing, (c) end of printing run.

4.2.7 Wet Print Thickness

As discussed in section 4.2.4, the wet print thickness depends on a variety of factors. Mesh count and wire diameter define open area of the mesh. This along with mesh angle, emulsion thickness, squeegee hardness, squeegee deformation angle, squeegee speed, ink viscosity and substrate roughness are among parameters that affect wet print thickness. Hence, it is very difficult to arrive at an accurate formula for wet print thickness. An estimate for wet print thickness (T) can be obtained from:

$$T = [\text{Average thickness of screen} \times \text{Percentage open area}] + \text{Emulsion thickness.}$$

The final thickness of the ink, after it is cured, will be less than the wet print thickness as the solvent evaporates during curing. The final thickness of the fired film depends on the percentage of vehicle and binder in the paste mixture.

4.3 Experiments

Screens of different mesh numbers 225, 250 and 325 with pre-coated emulsion (E-11, Sefar America) were used for screen printing. Since the minimum line width of the interconnect pattern in this work was 350 μm , most of the screen printing work was done using the screen of mesh count of 325. The screen was fitted in a metal frame of outer dimensions 14" \times 14" and inner dimensions of 12" \times 12" with a printable area of 9" \times 9". The emulsion was 0.6 mil thick, and the unexposed parts dissolved in water when developed. The screens were patterned by UV exposure. The wire mesh has a thread diameter of 36 μm and an equal spacing between threads, an open area of 50 % aligned at 90° to the frame.

Opti-Print 1616PD bench top screen printer shown in Fig. 4.2 was used in this work. The detail specifications are given in the Appendix.

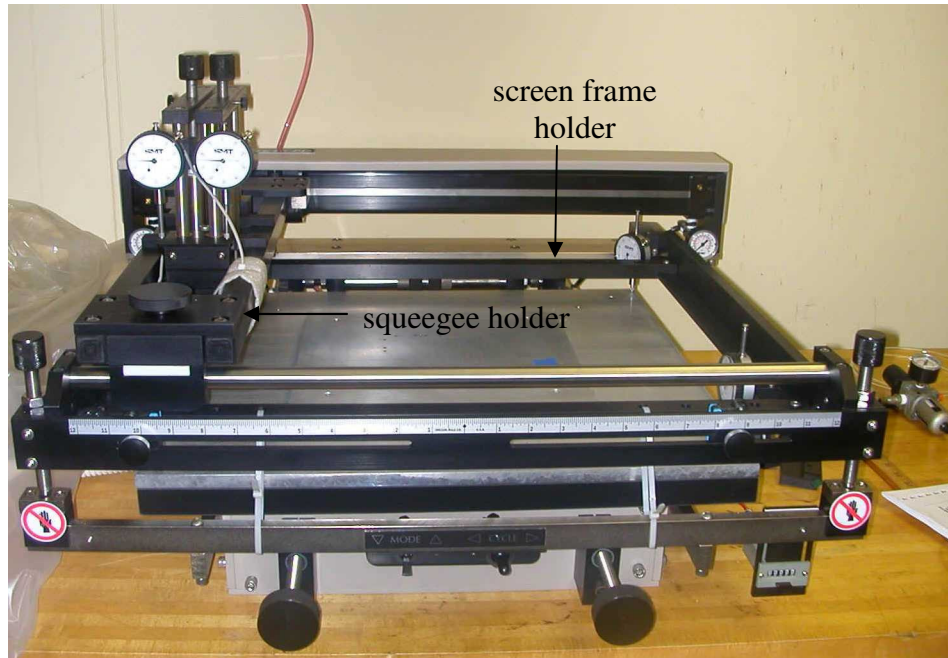


Fig. 4.2 Opti1616PD bench top screen printer.

An electrode pattern as shown in Fig. 4.3 was designed and printed. The end contact pad size is $1.4 \text{ mm} \times 1 \text{ mm}$, line width is 1 mm and spacing between lines is 1 mm . The pattern was designed in Auto-CAD and printed on a transparency using an office ink-jet printer, and used as a mask during exposure. It was transferred onto the emulsion of a mesh screen by exposing the emulsion with 360 nm UV light for nine and half minutes. The Exposure setup is shown in Fig. 4.4. The screen was mounted on a wooden frame and the transparency was clamped to it. The whole setup was placed at a distance of 1 meter from the UV light source such that one fourth of the screen is exposed at one time. At this distance, the intensity of light is 1.4 mW/cm^2 and only a fourth of the screen can be exposed. Since the pattern area of $1'' \times 0.75''$ is much smaller than the total printable area on the screen, the latter was divided into four with nitrogen and baked in an oven at $100 \text{ }^\circ\text{C}$ for 5 min . Figure 4.5 shows the process steps.

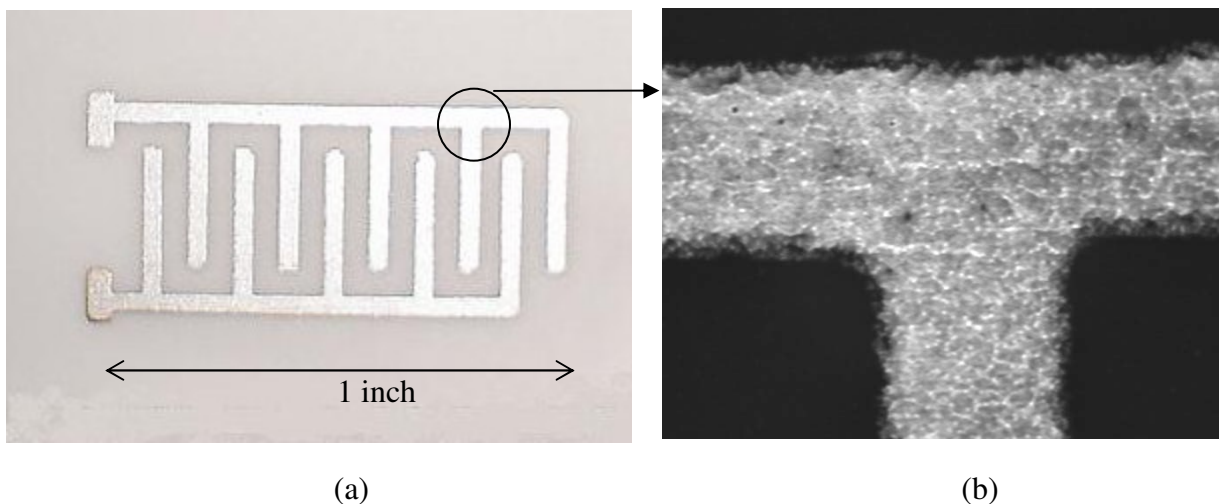


Fig. 4.3(a) Silver electrode pattern printed on a ceramic substrate. (b) Microphotograph of the printed electrodes.

The minimum line width that can be obtained in the mesh emulsion using the above setup depends on the resolution of the printer used to print the pattern on the transparency mask, and the manner in which the mask is mounted on the screen. Using the above described setup, a minimum line width of 250 μm was obtained on the mask. The metal electrodes were printed on alumina substrates which were cleaned in trichloroethylene at 60 $^{\circ}\text{C}$ for 5 min and then stored in methanol till used. Silver conductive inks ED3000 from Electrapolymers and 590-G from Electroscience, and carbon resistive ink R300 from Electroscience were used to initially characterize the printing process on the screen printer. The screen was set to print at various speeds and off contact heights at squeegee pressure of 80 PSI to determine the best possible printing conditions.

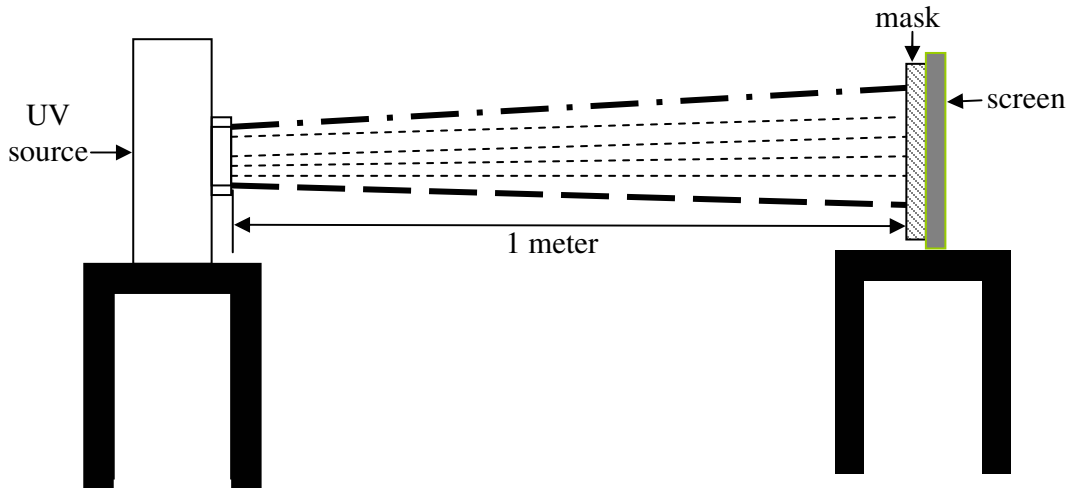


Fig. 4.4 Exposure setup.

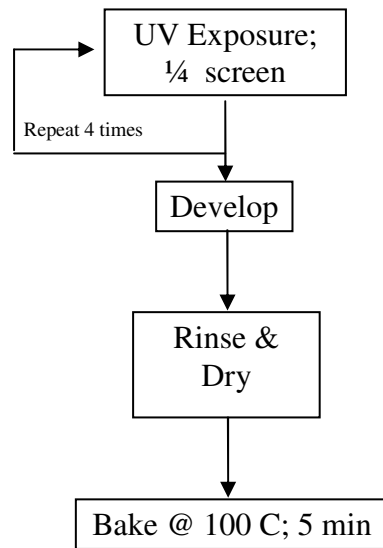


Fig. 4.5 Screen lithography process.

Off-contact height of 1, 2, 3, 4 and 5 mm and squeegee speeds from 1 cm/s to 5 cm/s were tried with squeegee pressure of 80 PSI. The print quality was good when resistive ink (R300) was used, but silver conductive ink (590-G) did not flow through the

open areas even at high squeegee pressures. This is due to the high viscosity of conductive ink 590-G. However, when ink 590-G was diluted with a thinner, good print quality was obtained. Figure 4.6 shows the variation of viscosity and shear stress with shear rate for silver conductive ink 590-G. The measurements were done using a Brookfield cone/plate viscometer. It can be seen that the viscosity of the ink decreases with the increase in shear rate. This drop in viscosity allows the ink to flow through the open areas of the screen mesh and deposit on the substrate. Silver conductive ink ED3000 has very low viscosity and its print quality was good at all speeds tried in this work. Off-contact height of 2 mm, squeegee speed of 2.2 cm/s and squeegee pressure of 80 PSI resulted in the best quality of print with no residual ink left in the open areas of the screen for both ED3000 and diluted 590-G silver conductive inks. After printing, the screen was cleaned with trichloroethylene to remove the ink remnants in the open areas, and blown

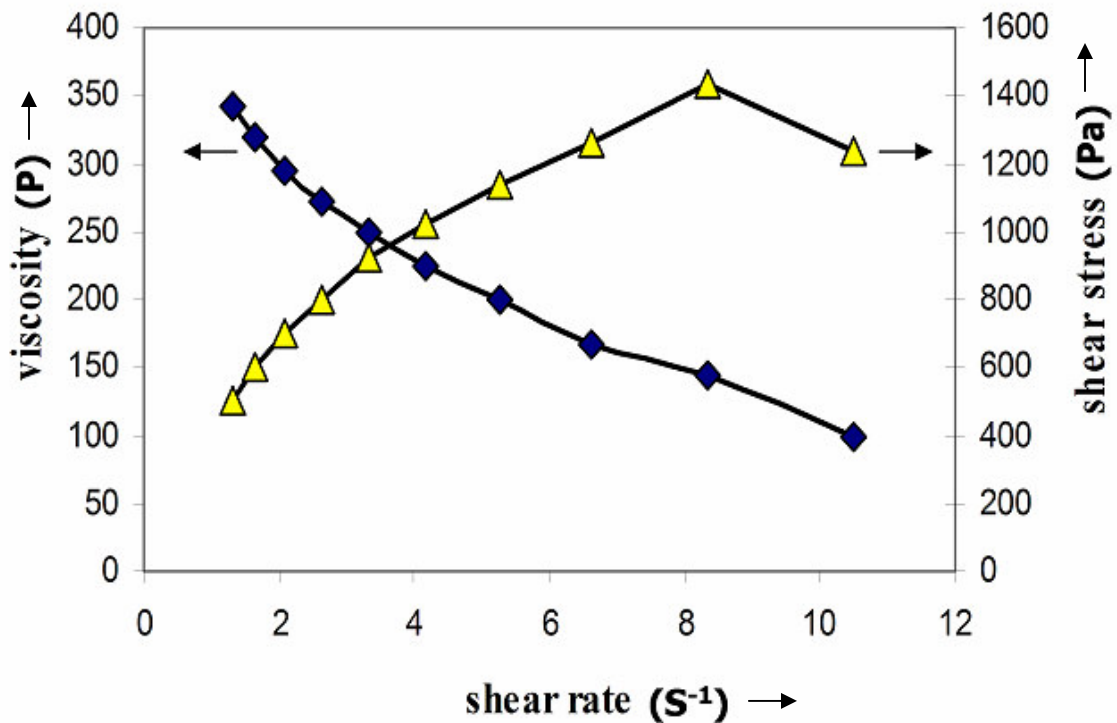


Fig. 4.6 Variation of viscosity and shear stress with shear rate for conductive ink 590-G.

dry with air. The substrate was allowed to dry in the air for 10 minutes prior to curing. The 590-G silver conducting paste films were cured at 450 °C for 30 minutes and those printed with ED3000 silver conducting ink were cured at 120 °C for 30 min. under atmospheric conditions. The thickness of the electrodes resulting after curing was approximately 13 μm for 590-G ink paste and 8 μm for the ED3000 ink as shown in Fig. 4.7. Figure 4.3(b) shows microphotograph of electrodes printed using 590-G ink. The thickness of the print is independent of the off-contact height [42].

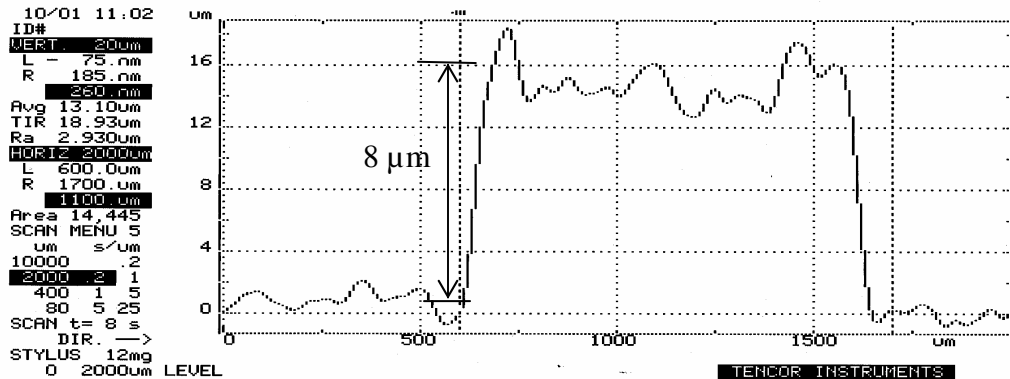


Fig. 4.7 Thickness of ED3000 silver conducting ink paste after curing.

After satisfactory screen printing parameters were determined, only ED3000 (Electrapolymers) was used for all subsequent printing owing to its low viscosity and low curing temperature. ED3000 ink was printed on ceramic, silicon, glass, polyvinyl sheet, 5 mils thick kapton 500 HN and 4 mils thick polyimide substrates. Kapton, polyimide and polyvinyl are flexible substrates and are not suitable for high temperature treatment above 250 °C, while ceramic, silicon and glass can withstand higher temperatures.

Polyimide substrate was made by spinning Pyralin 2611 from HD Microsystems at 750 RPM on a silicon wafer. The substrate was then heated on a hot plate at 150 °C for 5 min in air and then a second layer was spun at the same RPM and baked at 150 °C for 5

min. in air. The temp was then ramped to 350 °C at the rate of 4 °C/min and baked for 30 min at 350 °C. After the substrate cooled down, polyimide was peeled off the Si substrate and the peeled layer was used as a substrate for screen printing. While baking polyimide films, the temperature ramp up rate need to be controlled precisely to prevent formation of air pockets in the film. Thicker layers need to be spun to prevent curling up of polyimide film after being peeled off the substrate. The thickness of the polyimide film obtained using this recipe was 100 µm and the films did not curl up. The polyimide flexible substrate is bio-implantable as it has low water absorption coefficient. Figure 4.8 shows the electrode pattern printed on polyimide substrate using ED3000 silver conductive paste. The print quality with ED3000 conductive ink observed on polyimide substrate was good and its surface was free of pin holes. The thickness of the printed lines was found to be approximately 8 µm after curing the ED3000 conductive ink. The thickness was seen to be independent of the type of substrate used for six different types of substrates used. The quality of the print is dependant on the surface energy of the substrates. If the surface energy of the substrate is less than the surface tension of the ink, then the ink is attracted to the substrate and the print quality is good and fine printing can be obtained. All printing was done at a squeegee speed of 2.2 cm/s, off-contact height of 2 mm and squeegee pressure of 80 PSI. The films were allowed to dry for 10 min. prior to curing at 120 °C for 30 min in air.

4.4 Hybrid Integration

After the screen printing parameters to print on flexible and ceramic substrates were determined, the BESS chip integration was carried out. The printing ink used was ED3000 silver conducting ink. The most suitable printing parameters determined in the

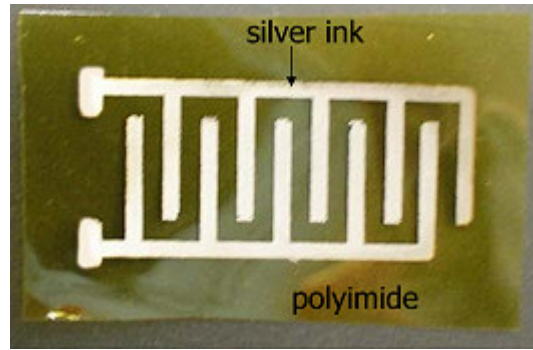


Fig. 4.8 Silver conductive ink printed on 100 μm thick polyimide substrate.

previous section were used. Squeegee speed of 2.2 cm/s, squeegee pressure of 80 PSI and off-contact height of 2 mm were used. The components that make up the BESS are shown in Fig. 4.9. The BESS IC, off-chip components and the receiver circuit need to be integrated in a 1" \times 0.75" area flexible substrate that can fit inside the receiver coil. The BESS chip circuit has to be printed on one side of the substrate and the receiver coil circuit on the other side of the same substrate.

The interconnect pattern was designed in Auto-Cad and printed on a transparency to be used as a mask to expose the screen. As discussed earlier, the minimum width that can be obtained on the screen emulsion using this set up is 250 μm , hence the interconnects were all designed to be 350 μm wide. The bonding pads for the IC are 500 μm^2 in area. The bonding pad area for surface mount components is kept the same as the connecting lead end area of the surface mount components.

Figure 4.10 shows the interconnect pattern designed in Auto-Cad. The square at the center houses the BESS IC while dark lines are the interconnecting metal lines terminating in bonding pads on which discrete components are to be mounted. The whole

pattern was printed on ceramic and kapton substrates first. Figure 4.11 shows the receiver coil circuitry and the battery charger circuit that recharges the batteries. The receiver coil circuit includes two diodes and two capacitors that form the voltage doubler circuit and compensation capacitor. Figure 4.12 shows the mask pattern for the receiver coil circuitry and the battery charging chip. Both patterns were transferred on to the mesh screen emulsion using UV exposures. The BESS interconnect pattern was printed on ceramic and kapton substrates.

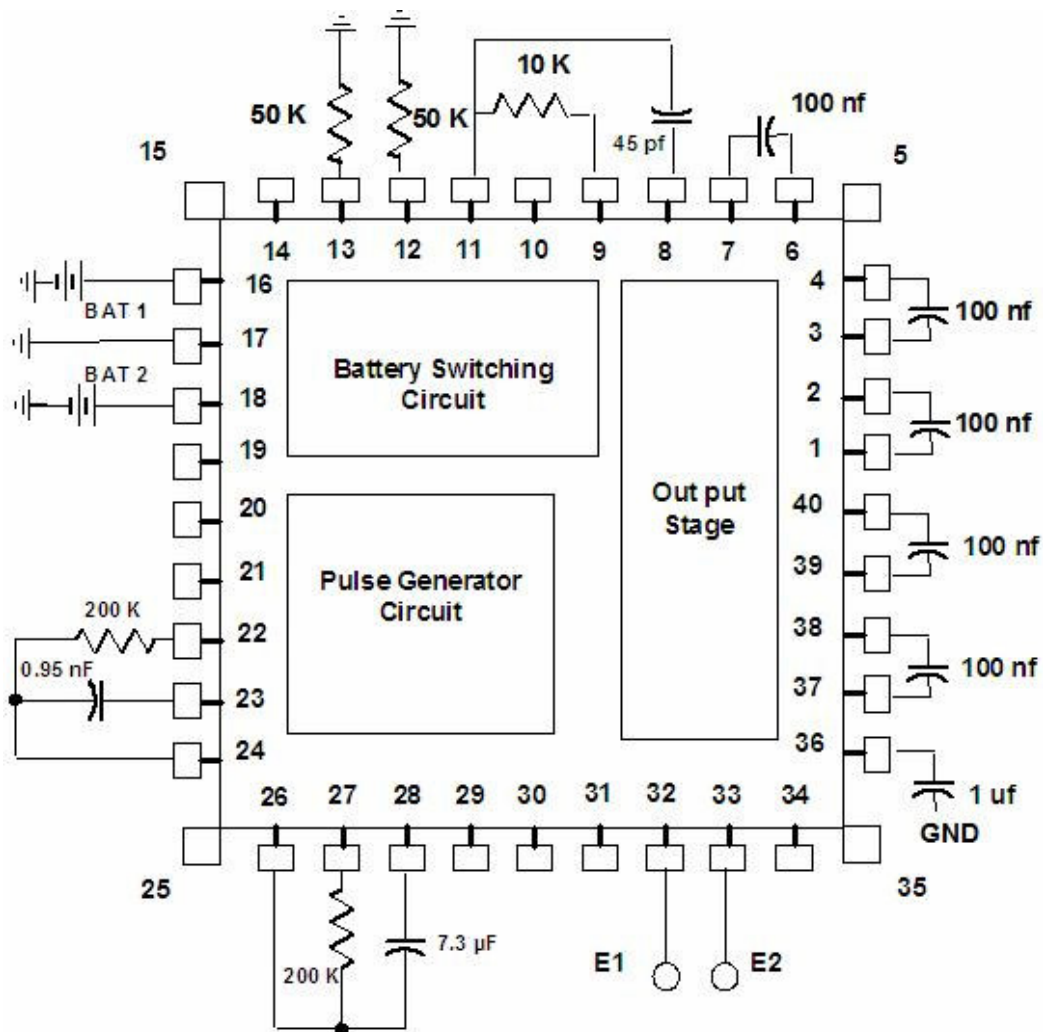


Fig. 4.9 BESS IC chip and required off-chip components.

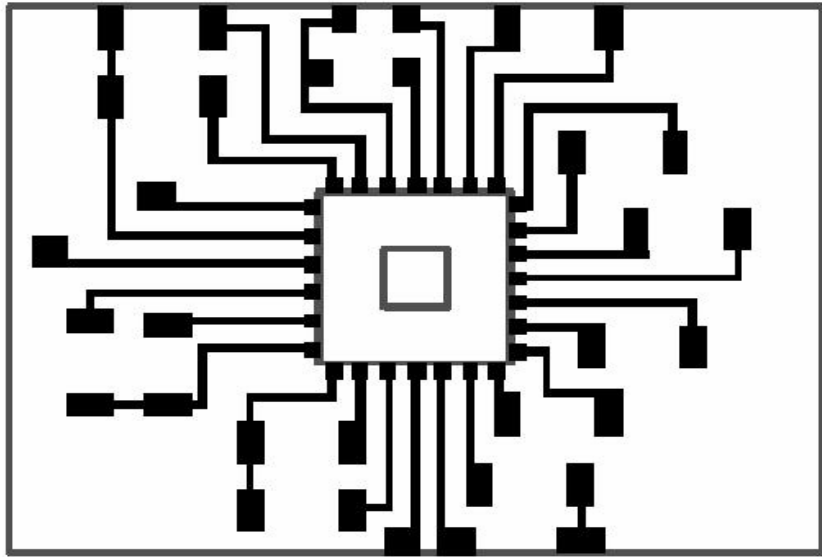


Fig. 4.10 Mask pattern for BESS integration designed in Auto-Cad. Size: 1" × 0.75".

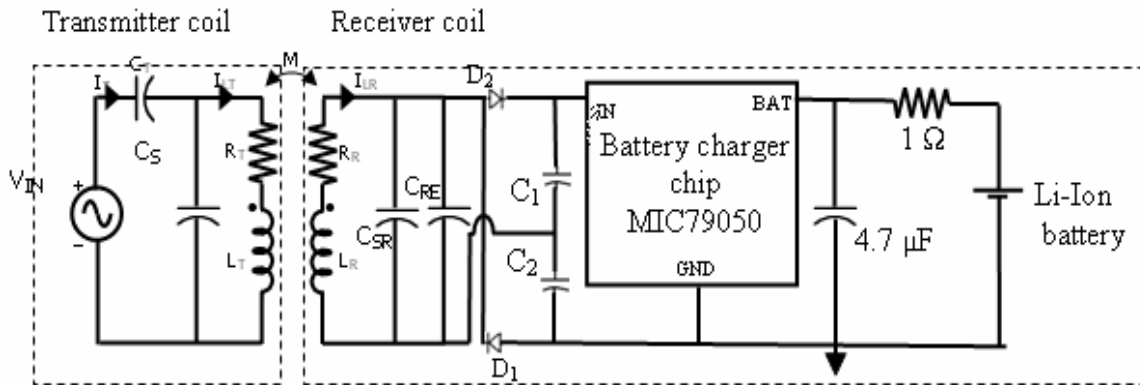


Fig. 4.11 Transmitter and receiver coil circuit for RPDS and battery charging chip. After reference [16].

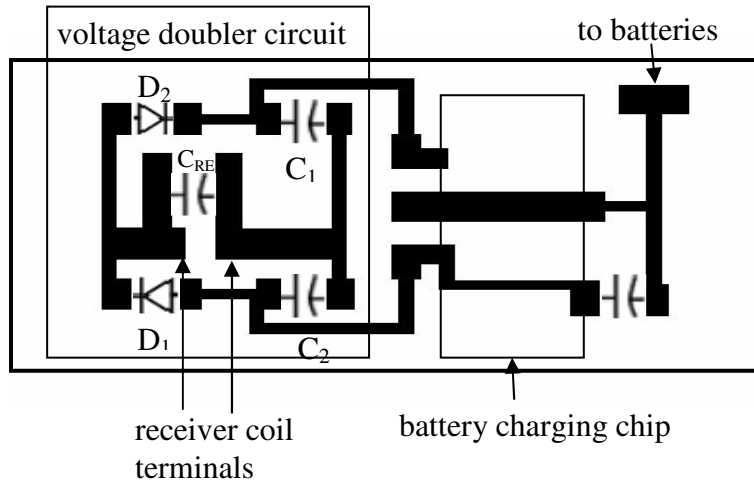


Fig. 4.12 Mask pattern for receiver coil circuit designed in Auto-cad. Size: 1" × 0.5".

4.5 Surface Mount Components

Figure 4.13 shows the BESS chip mounted on a bread-board, while Fig. 4.14 shows ceramic substrate with surface mount capacitors for hybrid integration with space in the middle for mounting the BESS chip. A two part silver conductive epoxy (CW2400, Circuit works) was used to mount the capacitors on the printed circuit. The epoxy was cured at 70 °C for 40 minutes. Conductive epoxy poses a challenge for its application on the bonding pads. The conductive epoxy need to be highly viscous so that it doesn't spread out, during drying and curing. If the epoxy spreads out, it could short circuit the components in a densely packaged integrated circuit. Usually the epoxy is applied by stencil printing, but it makes the screen cleaning process difficult. In this work, conductive epoxy was manually dispensed on the bonding pads and the capacitors were hand mounted. However, on visual inspection it was found that the smallest capacitors of 22 nF and 1 pF values were short circuited due to epoxy flow when cured. The capacitor sizes were 1 mm × 0.5 mm and distance between two lead ends is 0.5 mm.

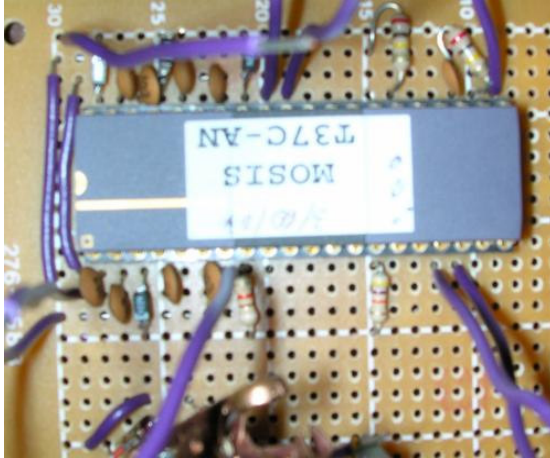


Fig. 4.13 BESS chip soldered with discrete components on a bread-board.

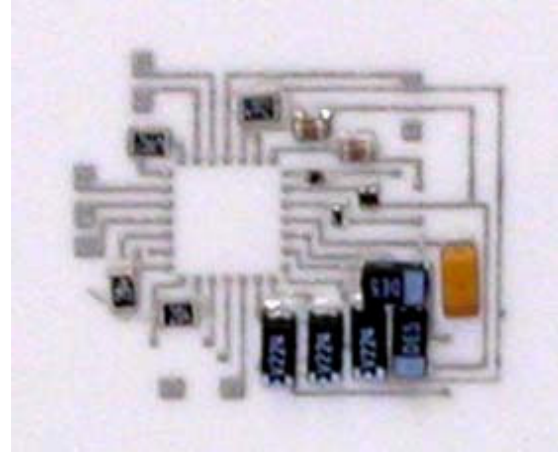


Fig. 4.14 Hybrid circuit on ceramic substrate with surface mount capacitors. Size: 1 in × 0.75 in.

The short circuiting problem due to epoxy flow was solved by mounting the capacitors on the bonding pads with a binder, and then dispensing the conductive epoxy in small quantities along the capacitor lead endings as shown in Fig. 4.15. However, these

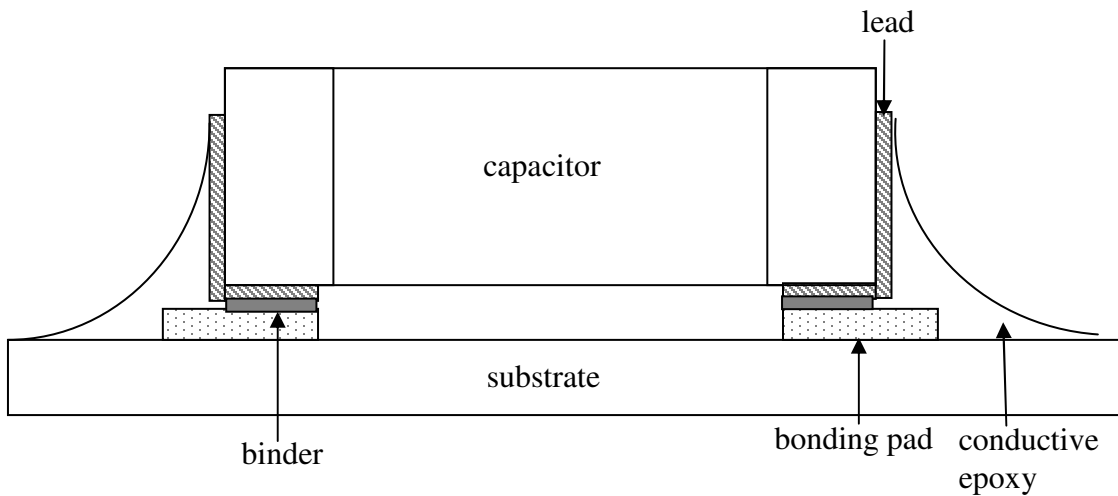


Fig. 4.15 Cross sectional view of a surface mount capacitor on bonding pad.

changes were not required as the BESS chip design itself was changed eliminating the need for small value capacitors. The changed design utilizes only 0.1 μF capacitors which are 3.2 mm long and 1.6 mm wide and could be mounted manually without shorting both terminals.

Finally, after the interconnect pattern is printed on the flexible substrate and the surface mount components bonded in place, the IC chip still remains to be integrated with the whole package. This will be done using an ultrasonic wedge bonder.

4.6 Summary

An electrode pattern to carry the output of the BESS IC chip and an interconnect pattern for packaging the off-chip components of the BESS IC chip and the receiver coil circuit of the BESS, were designed. Silver conductive inks ED3000 and 590-G were used to print the patterns. The screen printer was characterized to print at off-contact height of 1, 2, 3, 4 and 5 mm and squeegee speeds 1 – 5 cm/s at a squeegee pressure of 80 PSI. Good quality of print was obtained at squeegee speed of 2.2 cm/s, off-contact height of 2 mm and squeegee pressure of 80 PSI. Silver conductive ink ED3000 was preferred for its low viscosity. Screen mesh of count 325 with an open area of 50 % was used to print the interconnect pattern and electrode patterns. Electrode patterns were printed on ceramic, silicon, glass, kapton and polyimide substrates. The print thickness after curing was found to be 8 μm for ED3000 conductive ink and 13 μm for 590-G conductive ink. 100 μm thick polyimide substrates were prepared by spin coating pyralin at 750 RPM on a silicon substrate and baked at 150 $^{\circ}\text{C}$ for 5 min. A second layer was coated on it at 750 RPM and baked at 150 $^{\circ}\text{C}$ for 5 min and hard baked at 350 $^{\circ}\text{C}$ for 30 minutes before peeling it off the substrate. The polyimide substrates did not curl up upon peeling.

Electrode pattern was printed on this 100 μm thick polyimide substrate. The interconnect pattern for BESS IC chip was printed on ceramic and kapton substrates at a squeegee speed of 2.2 cm/s, off-contact height of 2 mm and squeegee pressure of 80 PSI. Surface mount components were hand mounted on the bonding pads using a two part conductive epoxy, and cured at 70 °C for 40 minutes. The epoxy flow problem which resulted in short circuiting small size capacitors was overcome by mounting surface mount components using a binder and dispensing epoxy along the capacitor lead ends. Mask pattern for receiver coil circuitry and the new BESS IC chip layout were designed in Auto-cad and screen mesh emulsion was exposed using UV exposure

5. SUMMARY AND SUGGESTIONS FOR FUTURE WORK

5.1 Summary

Pentacene thin films were deposited using thermal evaporation. Nickel contacts were used to measure the resistivity of the films. The films were deposited at a rate of 0.5 – 1 nm/s and annealed at 100, 150 and 200 °C for 30 minutes in nitrogen ambient. Resistivity was plotted as a function of temperature. It was observed that the resistivity decreased with the annealing. Defect activation energy of 0.22 eV was obtained from the curves. Grain size of the pentacene molecules was measured from the AFM images of the room temperature and annealed films. The room temperature deposited films have a grain size of 120 nm while pentacene films deposited at room temperature and annealed at 200 °C for 30 min in nitrogen ambient have a grain size of 150 nm. The grain size of the films did not show a marked increase after annealing.

Pentacene field effect transistors were fabricated on a heavily doped n-type silicon substrate. The substrate was coated with aluminum which acted as gate contact and 100 nm thick thermally grown silicon dioxide was used as dielectric. 150 nm thick Ni source and drain contacts were deposited on the silicon dioxide. Pentacene was evaporated over the nickel contacts through a shadow mask. The FETs have a W/L ratio of 4. Threshold voltage of 16 V and mobility of 0.0016 cm²/V-s was obtained from the I-V curves. The devices did not show saturation. Large W/L ratio FETs were also fabricated. However, these devices did not show any gate control over the drain current. The drain current varied almost linearly with the drain-source voltage. Threshold voltage of 1.5 V and mobility of 0.009 cm²/V-s was obtained for zero volt gate to source bias and W/L ratio of 400.

Contact resistance at the source and drain metal-semiconductor interfaces and schottky barrier at the interfaces along with the effects of device structure, annealing and doping were discussed.

In the later part of the thesis, a hybrid integration process was developed to package a Bio-implantable Electrical Stimulation System (BESS). The BESS is a gastric pacer system which generates pulses at a given amplitude and frequency to stimulate the gastric muscles. It consists of an application specific IC powered by rechargeable batteries. The batteries are charged by a remote power delivery system. The BESS IC, off-chip components, receiver coil circuitry and the batteries all need to be integrated on a flexible implantable substrate.

Screen printing was utilized to print the interconnect pattern of the BESS IC chip. Screen printing process was optimized to print at a speed of 2.2 cm/s, off-contact spacing of 2 mm and squeegee pressure of 80 PSI. Screen mesh count of 325, open area of 50 % and emulsion thickness of 0.6 mils were used for printing. These printing parameters were used throughout this work. Silver conductive ink ED3000 and 590-G were used. Good quality print was achieved on ceramic, silicon, glass, kapton and polyimide substrates using ED3000 silver conducting ink. The ED3000 ink films were cured at 120 °C for 30 min. The films have a thickness of 8 μm. The polyimide substrate, which is bio-implantable, was prepared by spin coating two layers of pyralin on a silicon substrate at 750 RPM and baking at 350 °C for 30 minutes. The thickness of the film was found to be 100 μm. Electrodes of ED3000 silver conducting ink were printed on the polyimide substrate to carry the output from the BESS IC to the gastric muscles. The interconnect pattern for integrating the off-chip components of the BESS to the IC was screen printed

on ceramic substrate and kapton substrate. The pattern occupies an area of 1 in × 0.75 in, small enough to fit inside the receiver coil. Miniaturized surface mount capacitors and resistors were hand mounted on the substrate using a two part conductive epoxy and set at 70 °C for 40 min. Mask pattern for receiver coil circuitry was designed in Auto-cad and the pattern was transferred on to the mesh screen using UV exposure. The BESS system is now ready for hybrid integration and system testing.

5.2 Suggestions for Future Work

There are several areas in which the organic field effect transistors and hybrid packaging can be improved. Few of them are detailed below. The performance of the organic field effect transistors entirely depends on the deposition process. Thermal evaporation is ideal for depositing pentacene, but to achieve repeatable results and higher mobilities the deposition rate need to be precisely controlled. Deposition rate determines the crystallinity of the deposited pentacene films. Purification of the starting material will also help in obtaining highly ordered films.

Pentacene is sensitive to chemical treatment. This places a limitation on the deposition of active material while fabricating the FETs. Pentacene is usually the last layer to be deposited and bottom contact configuration is the most convenient configuration. Shadow masks are used during the deposition of pentacene which makes alignment difficult. Also, to minimize fringing currents, it is desirable to deposit pentacene only over the area between the metal contacts. Shadow mask cannot achieve this. Thus, developing a chemical process for patterning organic semiconductors will help improve the performance of the organic FETs.

Since the BESS IC chip and receiver coil has to be bio-implanted, the bio-compatibility of the system needs to be investigated. The bio-compatibility of the packaging is an important issue. Bio-compatible packaging materials like titanium and PDMS have to be investigated to encapsulate the receiver coil. It is hoped that the initial hybrid packaging of the BESS will be a starting point to a more robust hybrid bio-implantable system.

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APPENDIX: SCREEN PRINTER SPECIFICATIONS

Opti-Print 1616PD bench top semi-automatic screen and stencil printer with dual independent squeegee system and 4 Point frame adjustment was used in this work. The following are the features of the screen printer.

Maximum Printing Area: 16" x 16"

Maximum Frame Size (OD): 23" x 23"

Maximum Off-contact: 1"

Maximum Cycle Speed: 10 - 12 sec

Print Speed: 0-14"/sec

Squeegee Pressure: 80 lbs. maximum

Squeegee Driver Force: 315 lbs.

Squeegee Holder Size: 7" Standard

Squeegee Angle: $\pm 7^\circ$

Platen Size: 21" x 22"

Platen Movement X & Y: 1"

Platen Rotation: $\pm 8^\circ$

Air Consumption: 100 PSI @ 1 CFM

Machine repeatability: $\pm 0.00025"$

VITA

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